

MS-7C26

Version : 1.0

CPU :

AMD AM4

System Chipset :

AMD PROMONTORY

On Board Chipset :

Intersil 6377HRZ 6Phase

Gigabit LAN -- RTL8111GN/RTL8111EPV

HDA Codec -- Realtek ALC662VD

Super I/O ---IT8738E

SPI Flash 256Mb

Main Memory :

2 Channel DDR 4 * 4 (Max 64GB)

Expansion Slot :

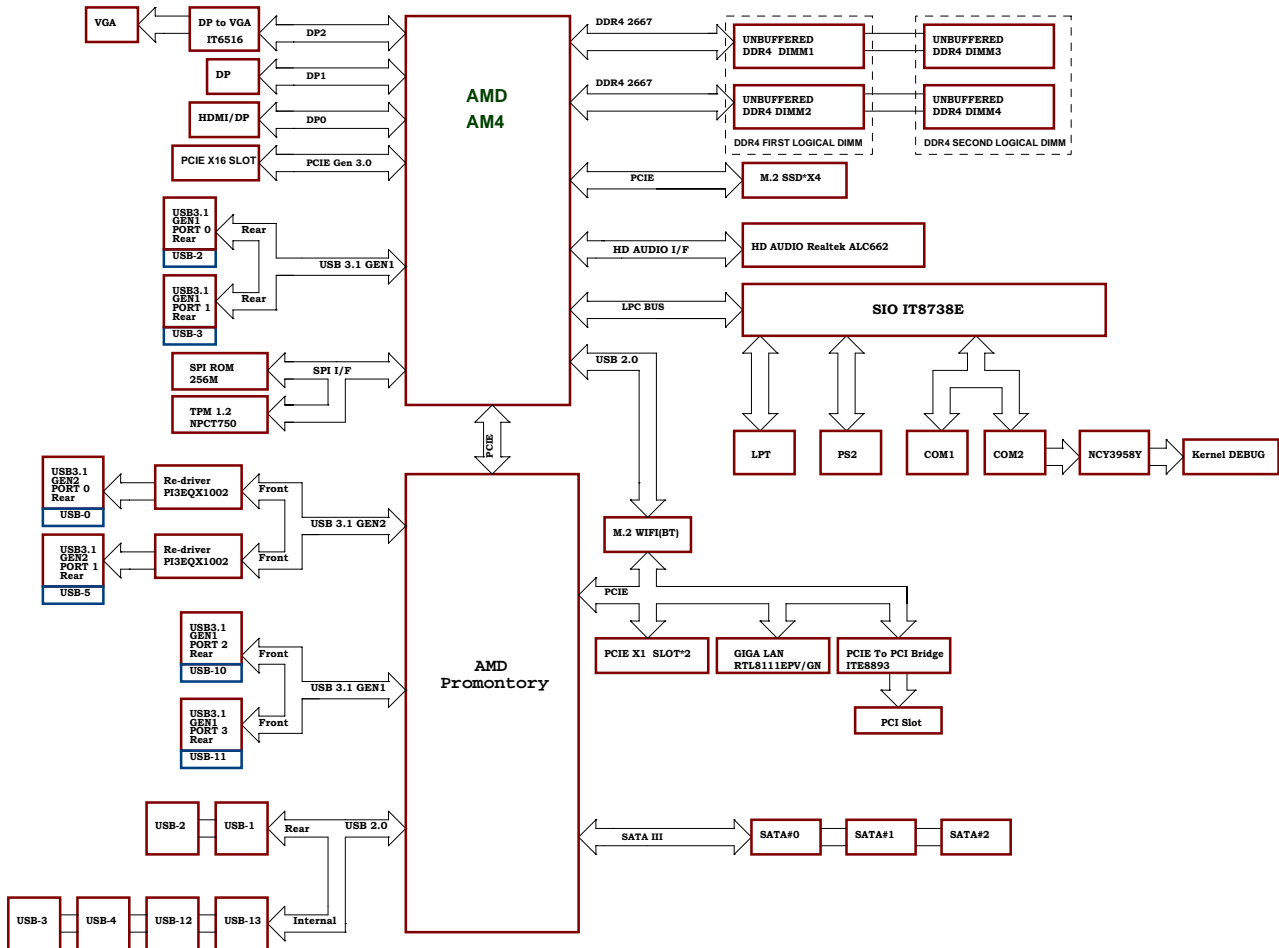
PCI Express x16 Slot * 1

PCI Express x1 Slot * 2

PCI Slot * 1

lenovo

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Slot Sequence:

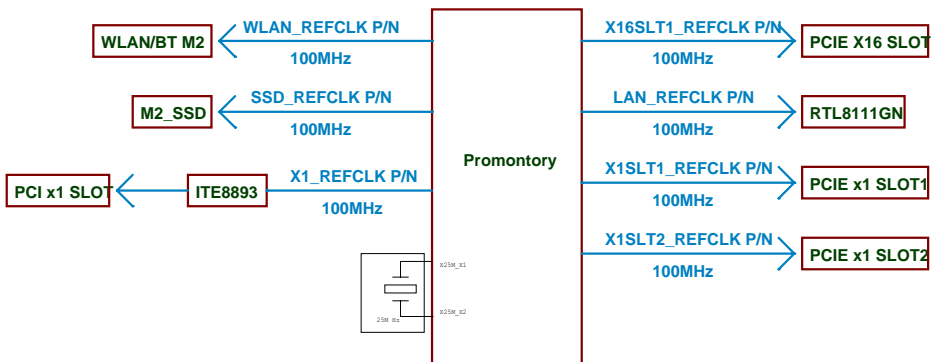
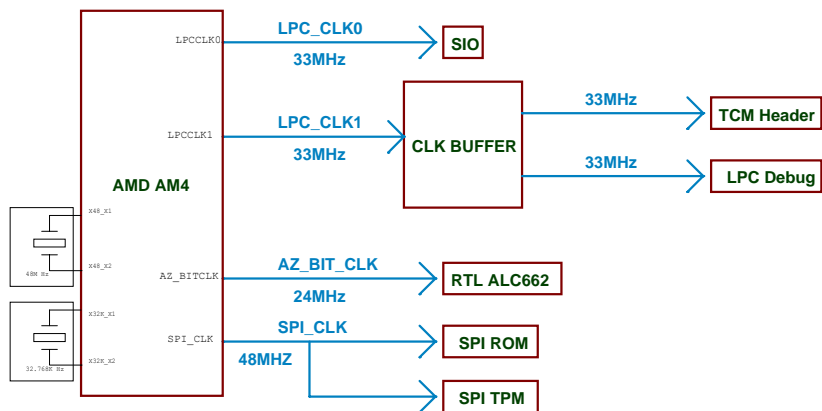
PCIE X16

PCIE X1

PCIE X1

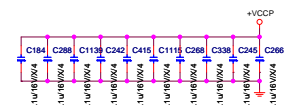
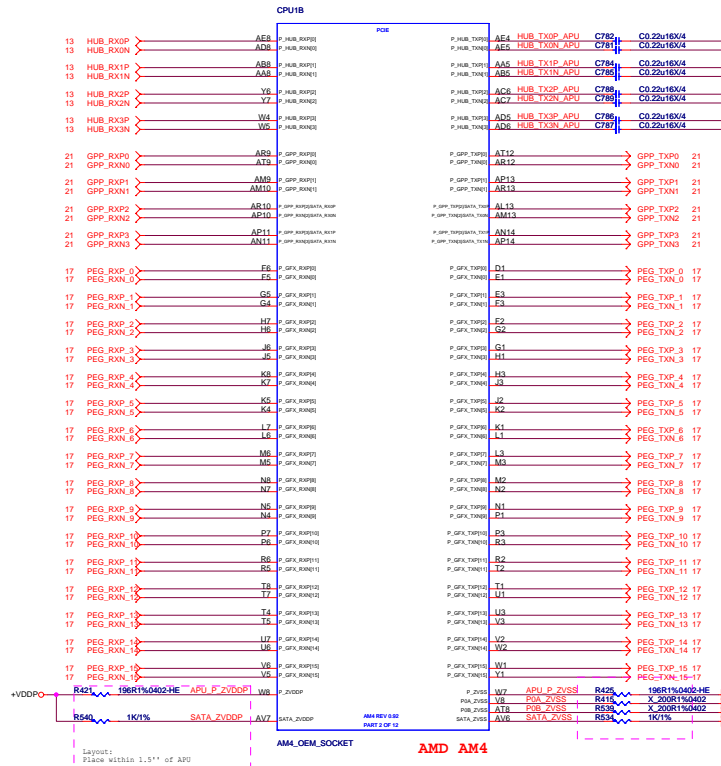
PCI

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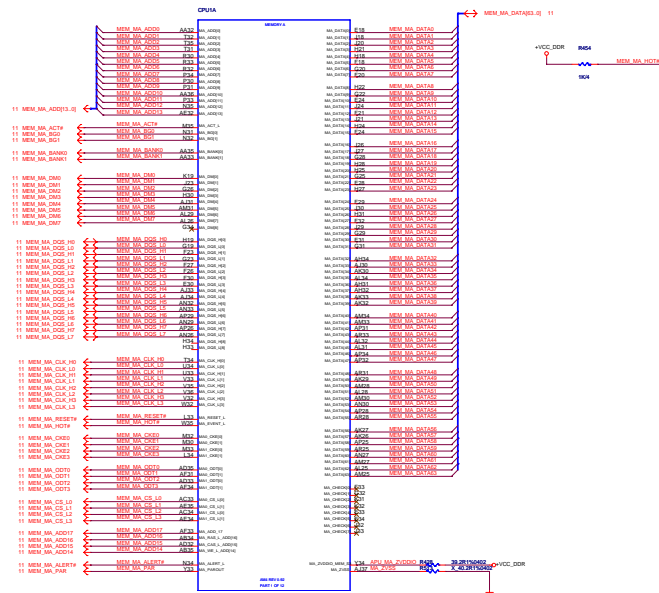


AM4 PCIE I/F

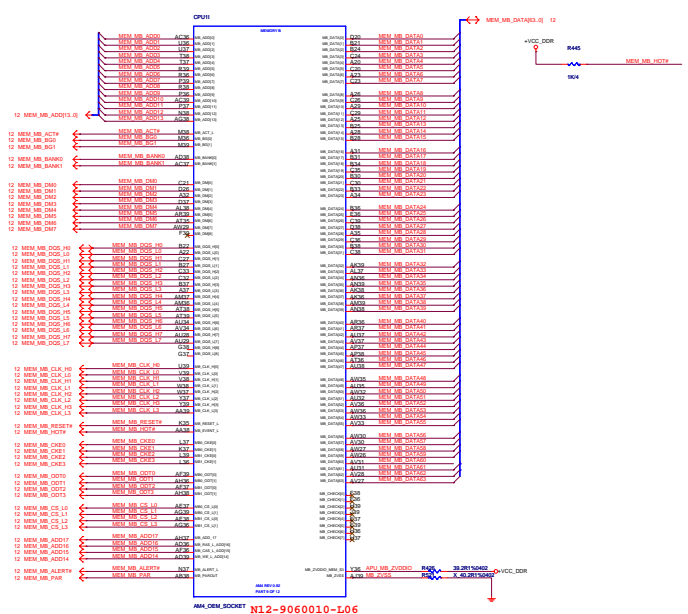
PCIE 3.0
Allowable Range: 176 to 265 nF
Recommended Value: 220 nF



AM4 DDR4 V/F(A)



AM4 DDR4 V/F(B)



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Layer81 Place within 1.5" of APU

APU RST#

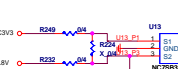
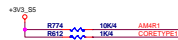
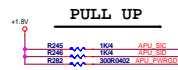
APU PWRO#

C243

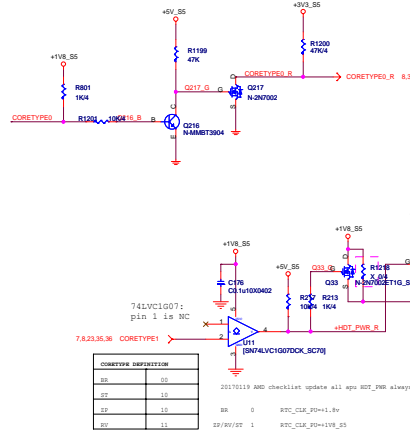
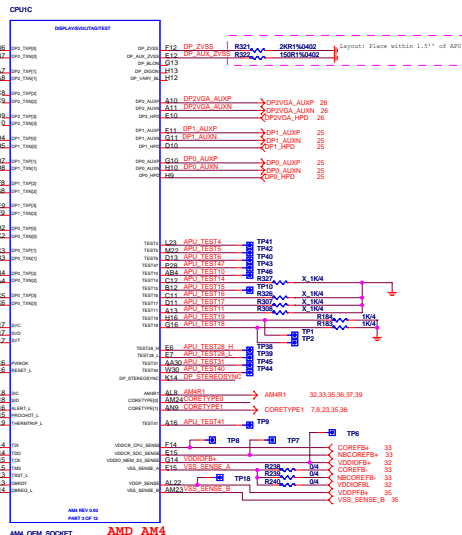
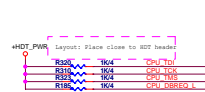
C206

C 30pF040402

C 30pF040402



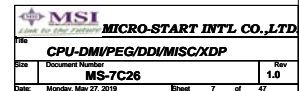
	CORETYPE 1	Function	PIN4
Type 0	0	S2 Connected to D	Pull high to +1.8V
Type 2	1	S1 Connected to D	Pull high to #VCC3V3
Type 3	1	S1 Connected to S	Pull high to #VCC3V3

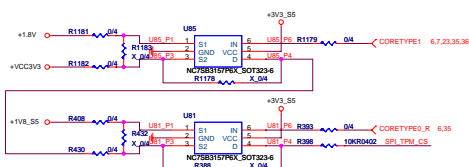
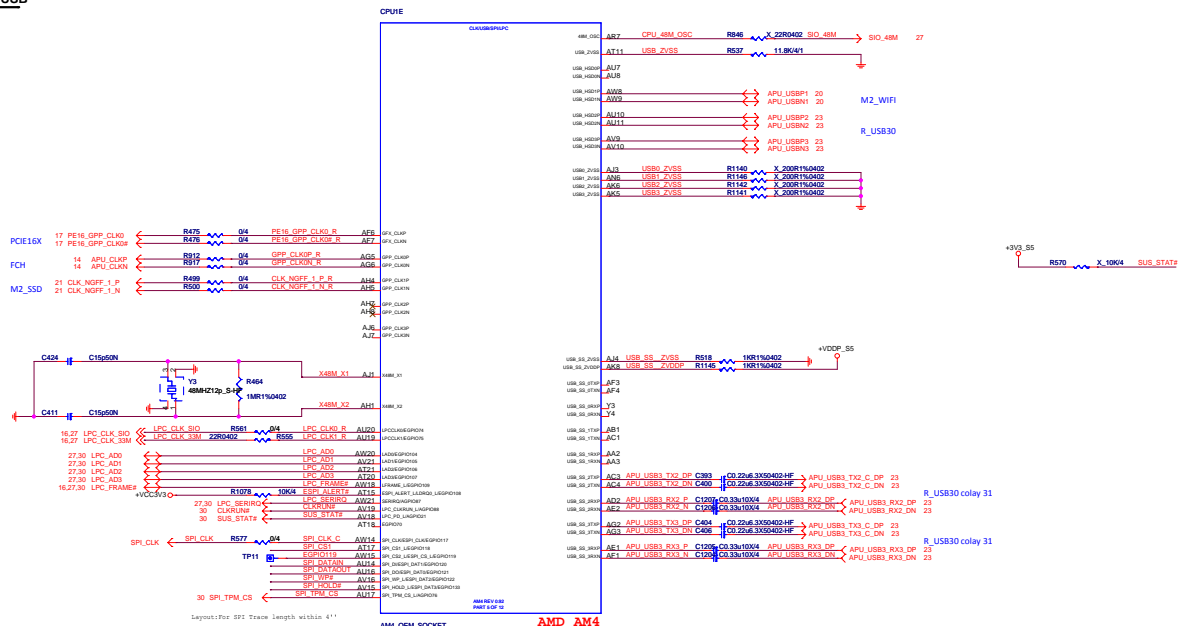


The diagram illustrates the CPU power supply network. A +1.8V supply is connected to a network of resistors and capacitors. The resistors are labeled R274, R259, R262, R258, R272, R273, R275, and R212. The capacitors are labeled X_2_200u4, X_1004, X_1004, X_200u4, X_200u4, X_200u4, X_200u4, and X_200u4. The diagram also shows connections to the CPU pins: CPU-PIN 6, CPU-PIN 8, CPU-PIN 9, and CPU-PIN 14. A label 'CPU PWING' is present.

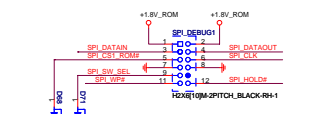
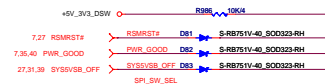
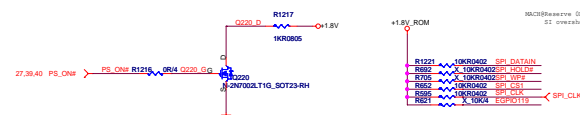


CORETYPE1	CORETYPE2	Family/Model Numbers	ARM Processor Type
0	0	Family 15h/Models 60h-6Fh	Type 0 Bristol
0	1	Reserved	Type 1
1	0	Family 17h/Models 00h-0Fh	Type 2 Summit
1	1	Family 17h/Models 10h-1Fh	Type 3 Raven

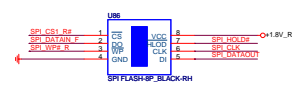
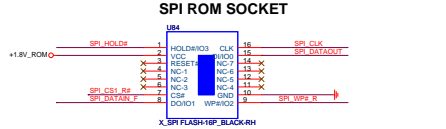
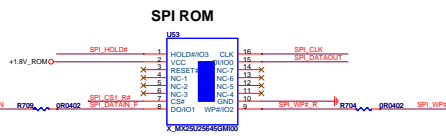




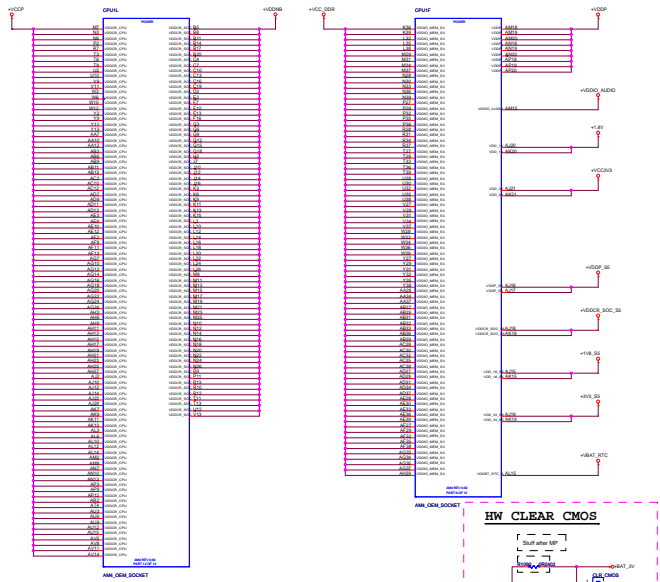
	CORETYPE 0	CORETYPE 1	Function	PIN4
Type 0	0	0	U85 S1 Connected to D	Pull high to +VCC[V3]
Type 2	0	1	U85 S1 Connected to D	Pull high to +1.8V
Type 3	1	1	U81 S1 Connected to D	Pull high to +V8[5]



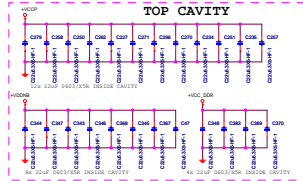
Remove after MP



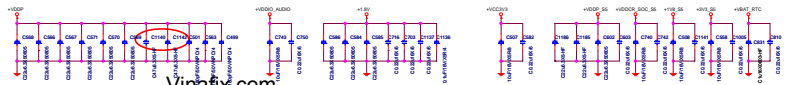
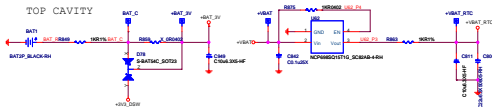
AM4 POWER



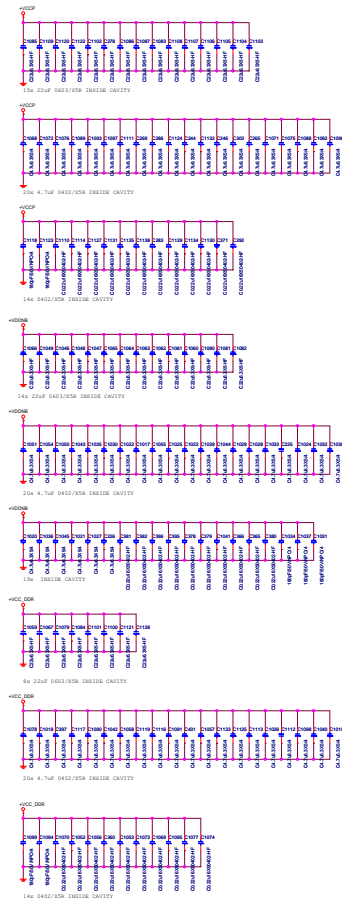
TOP CAVITY



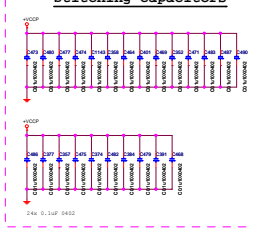
TOP CAVITY



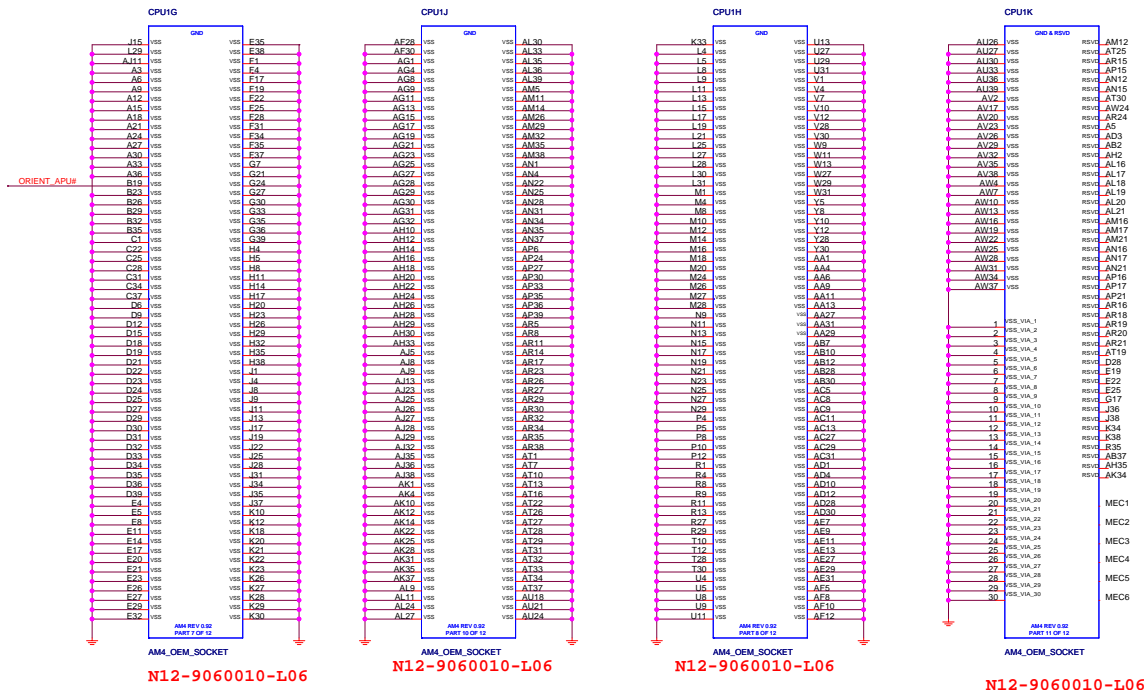
BOTTOM SIDE DECOUPLING

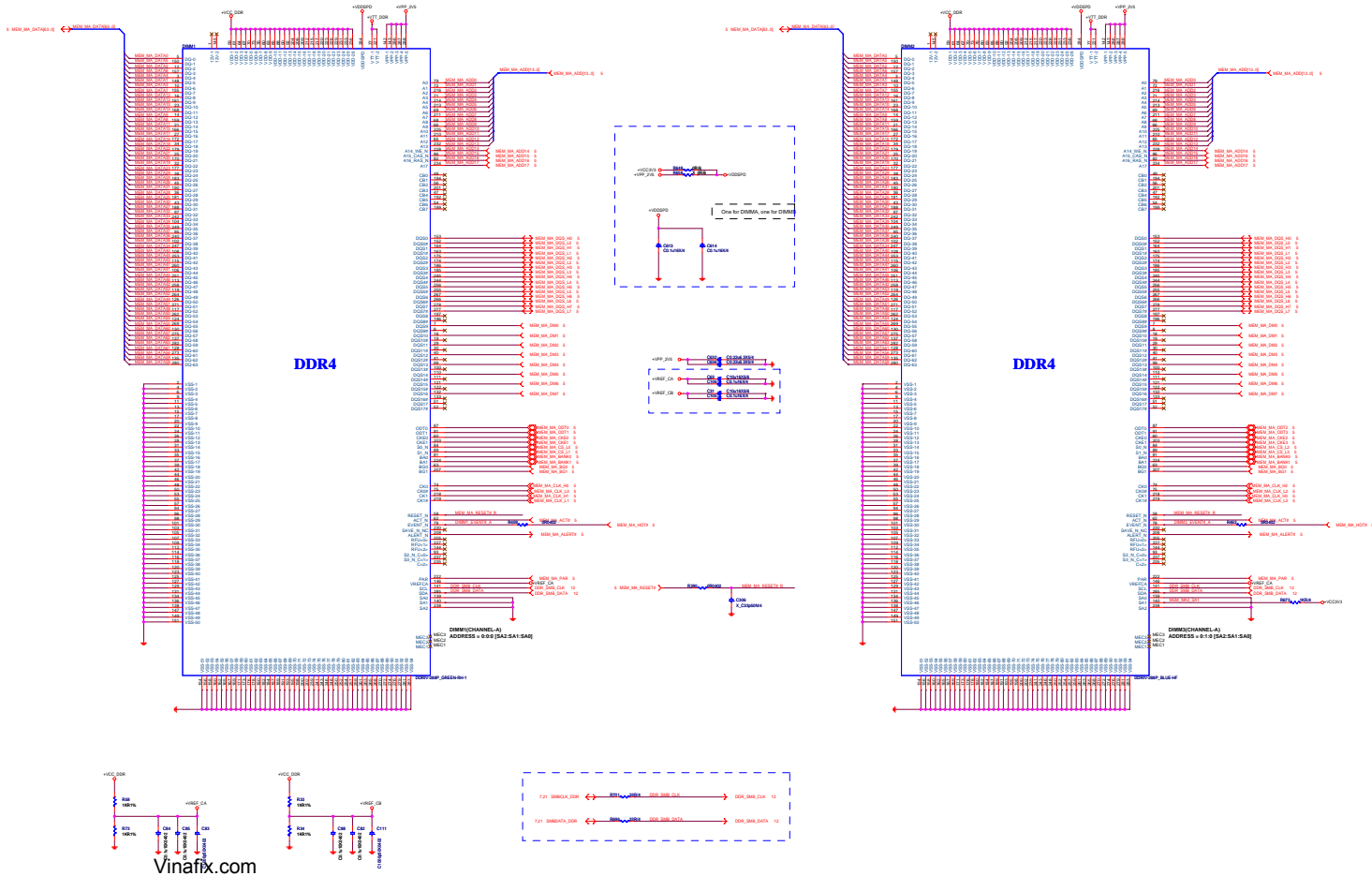


Stitching capacitors

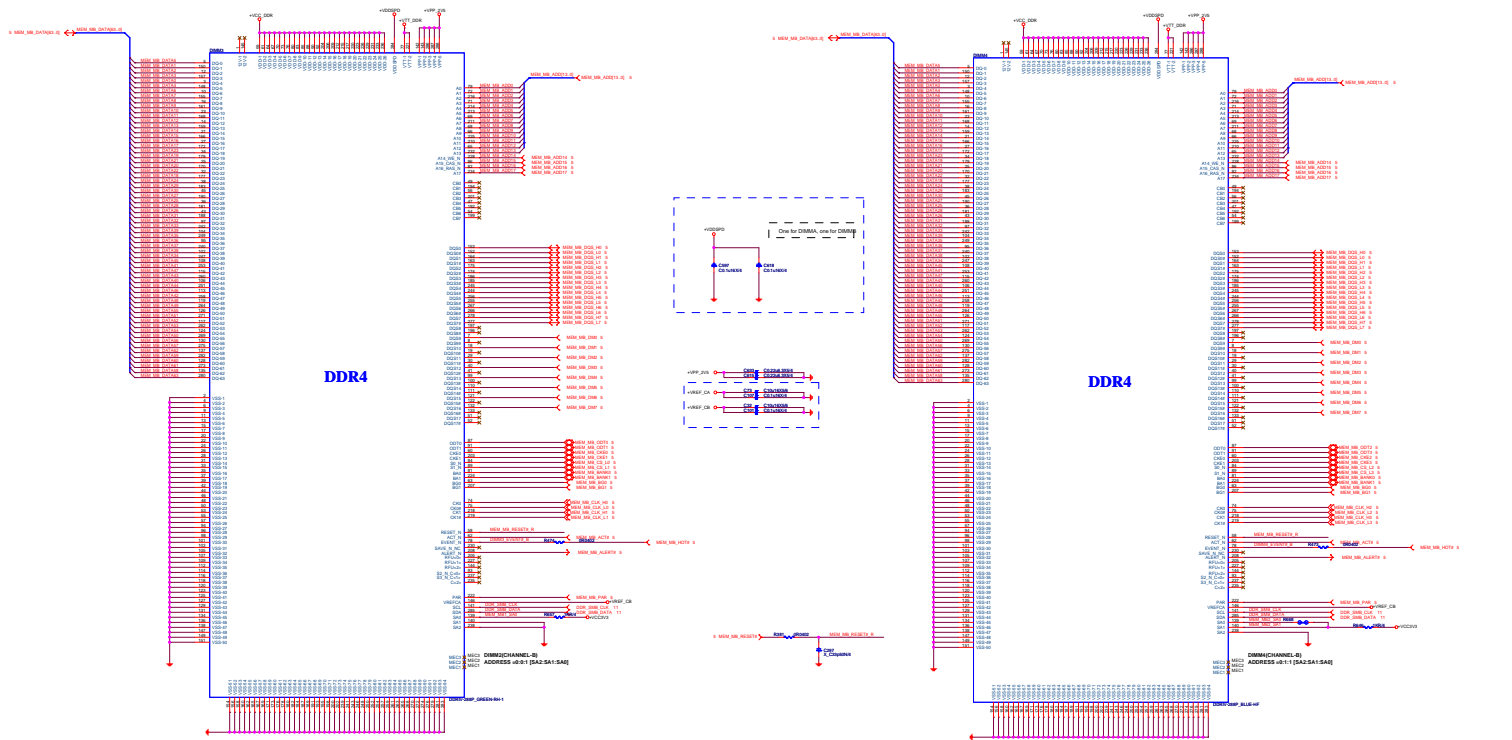


AM4 GND





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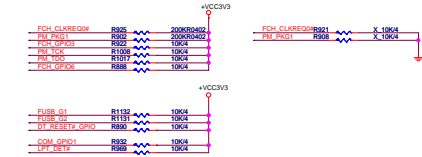
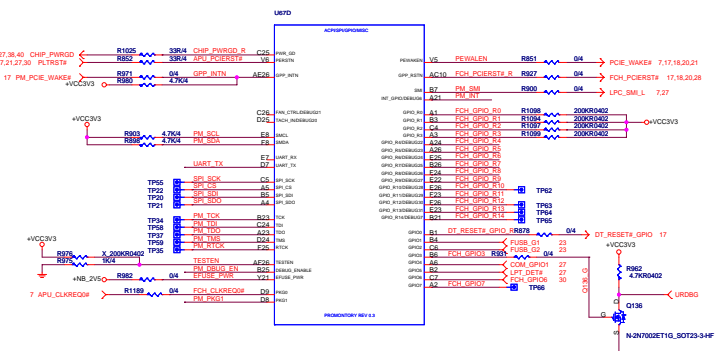
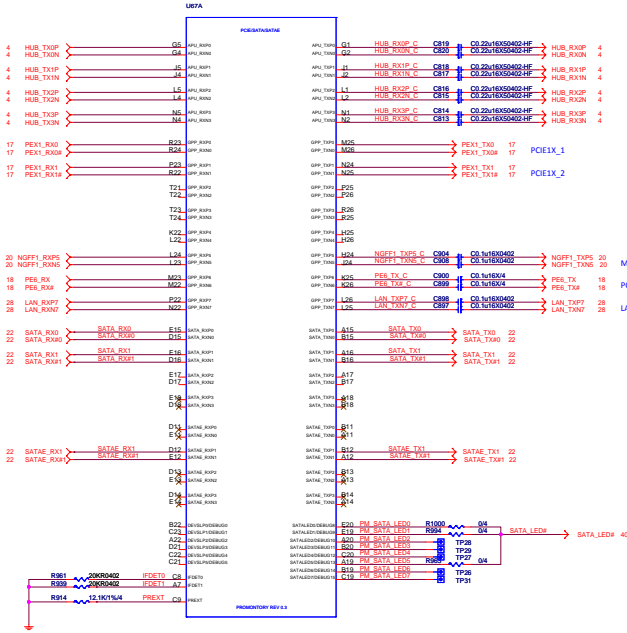


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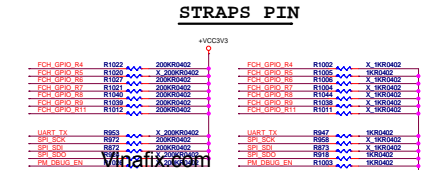
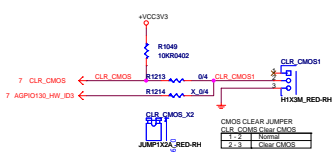
PROMONTORY PCIe/SATA/GPIO

PROMONTORY

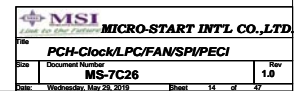
PROMONTORY



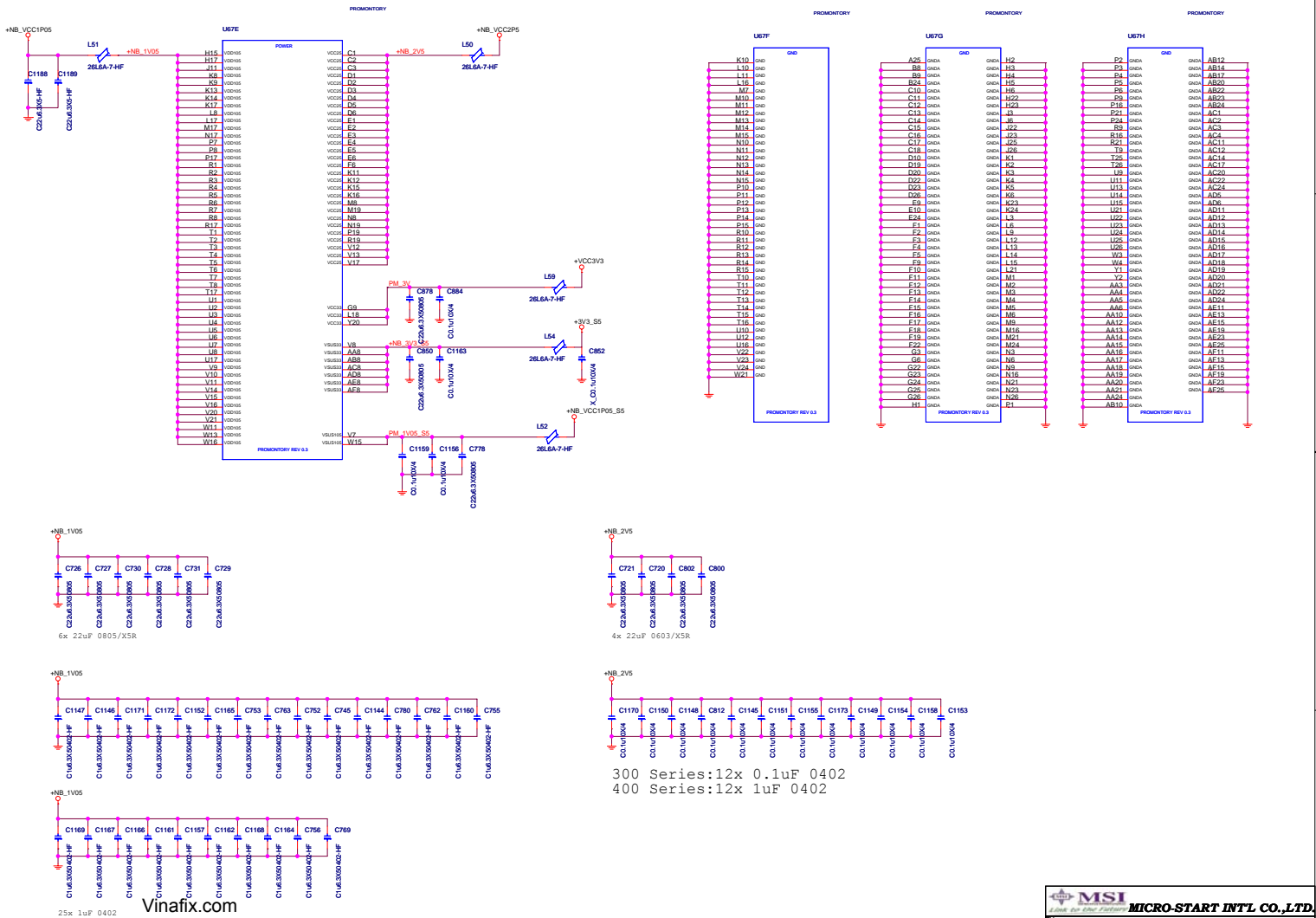
CLEAR CMOS



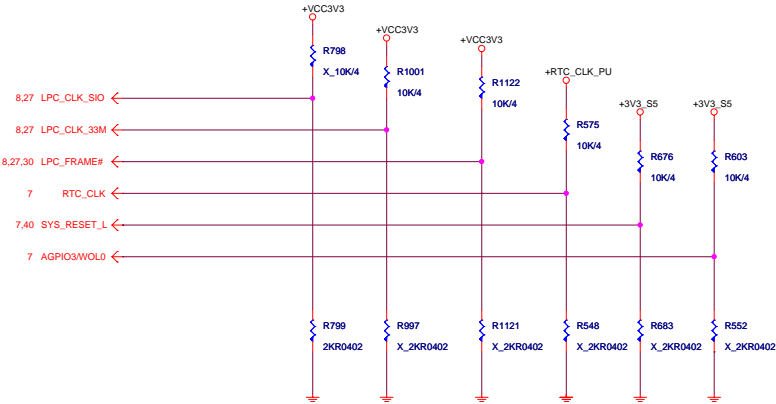
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PROMONTORY POWER

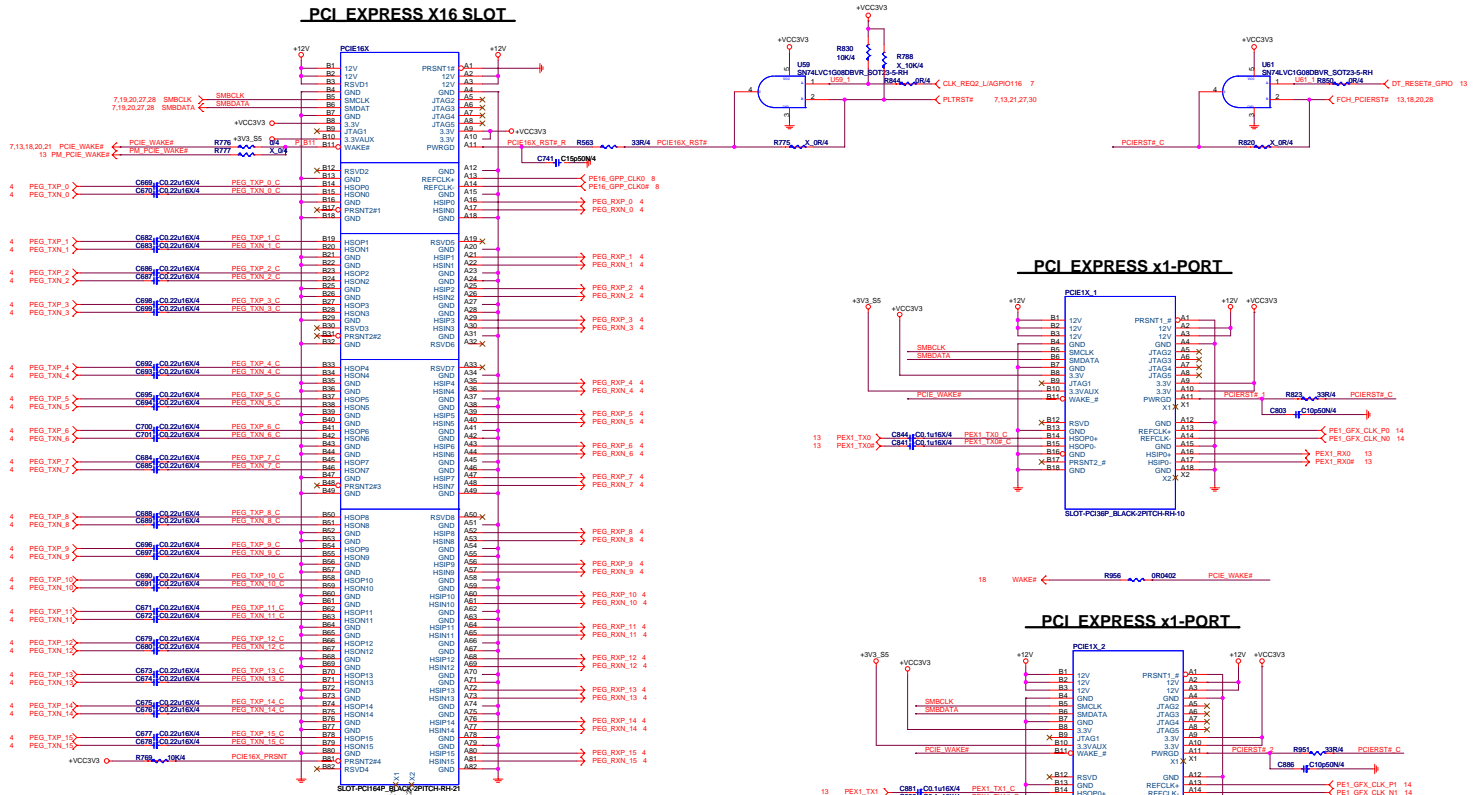


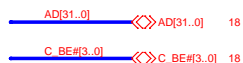
REQUIRED STRAPS



	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI CLK (ZP)
FULL HIGH	BOOT FAIL TIMER ENABLED	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48Mhz crystal clock and generate both internal and external clocks (DEFAULT)
FULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic	Coin battery is not on board.	LPC ROM	short reset mode	Use 100Mhz PCIE clock as reference clock and generate internal clocks only
CZ/ST DIE ONLY						ZP DIE ONLY	

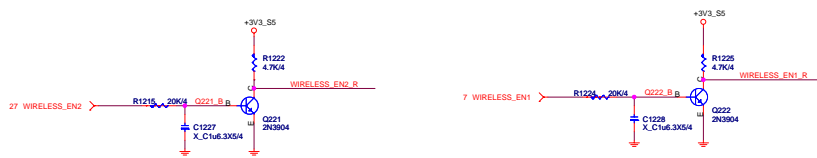
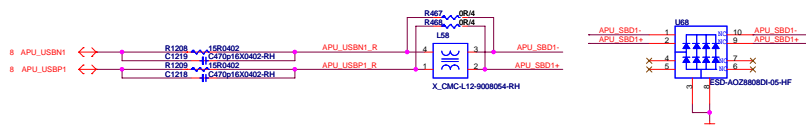
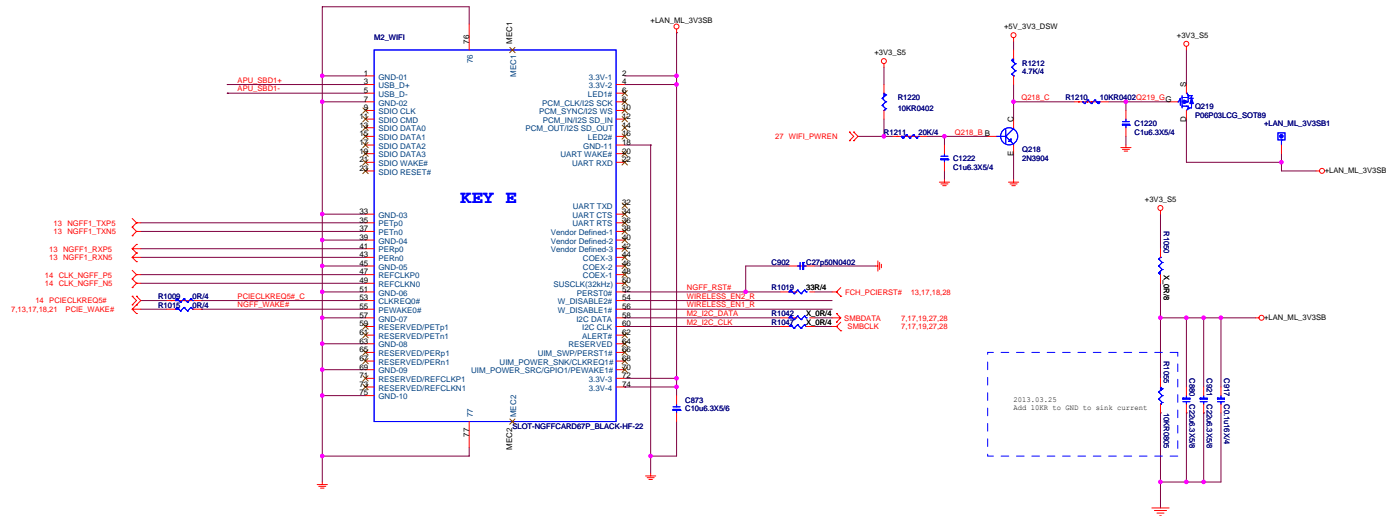
PCI EXPRESS X16 SLOT



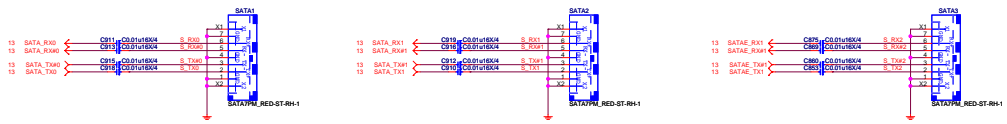


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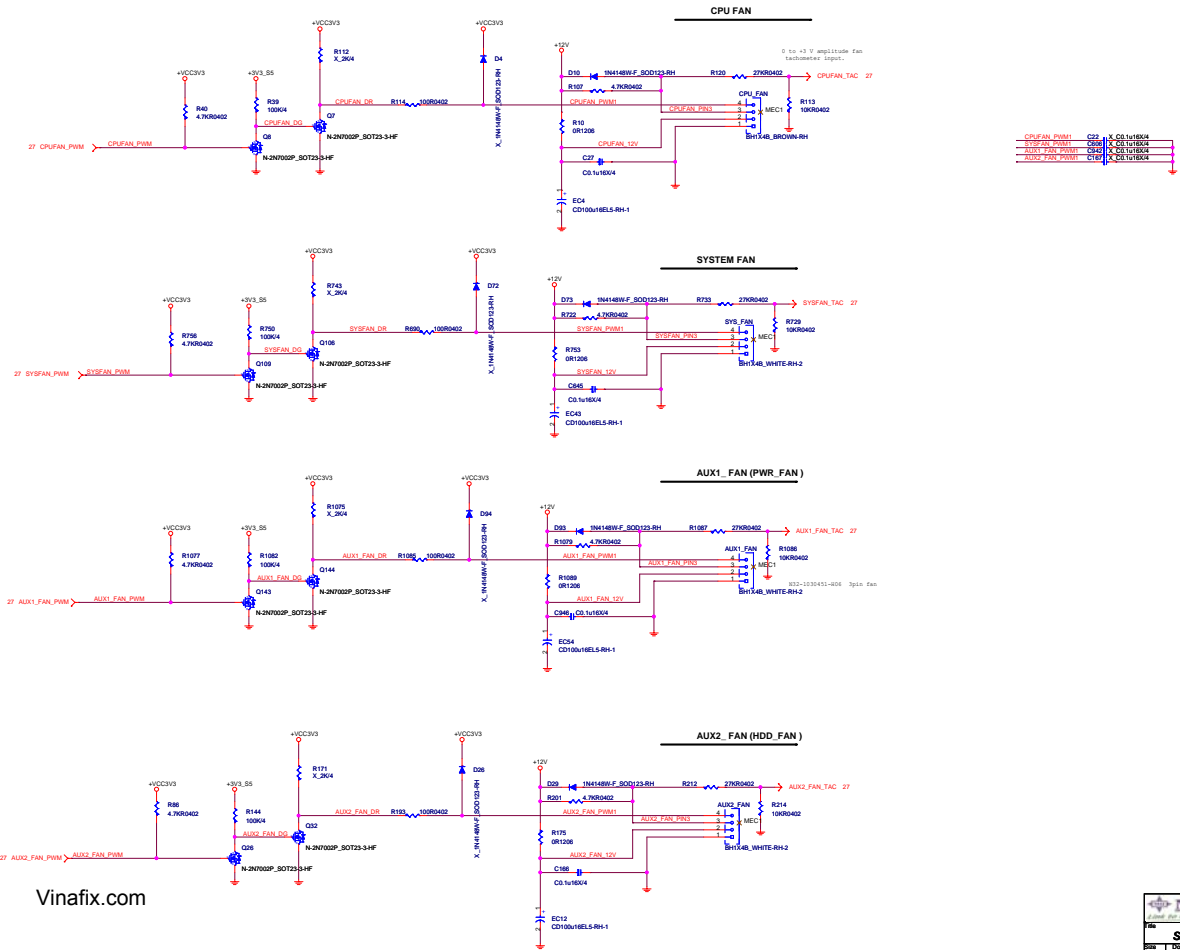
The schematic diagram illustrates the power supply section of the PCIRST# board. It features four input rails: +VCC5, +VCC3V3, +3V3_S5, and +12V. Each rail is connected to a series resistor (CR82, CR87, CR87, CR87) and a parallel combination of a capacitor (CQ25, CQ89, EC05, EC05) and a diode (C4706, C4706, C4706, C4706). The output of the +12V rail is labeled PCIRST#.



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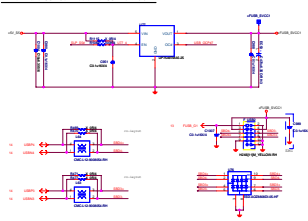


CPU FAN /SYSTEM FAN /POWER FAN

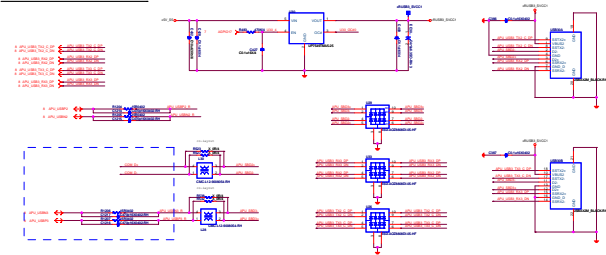


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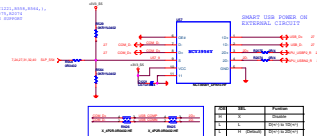
Front Panel USB Connector For USB Port 2/3



Rear Panel USB Connector For USB Port 3/4

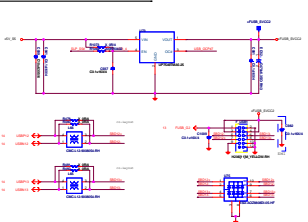


SWAP USB POWER ON
EXTERNAL CONNECT

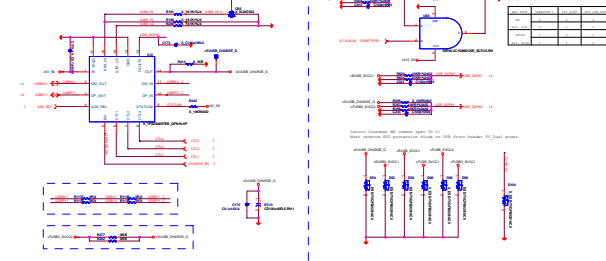


Pin	Signal	Function
1	VBUS	POWER
2	D-	DATA
3	D+	DATA
4	GND	GROUND

Front Panel USB Connector For USB Port 1

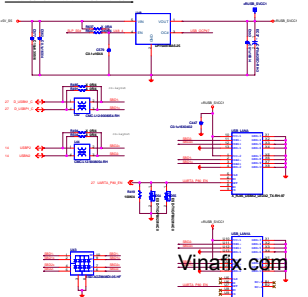


USB2.0 With Charge

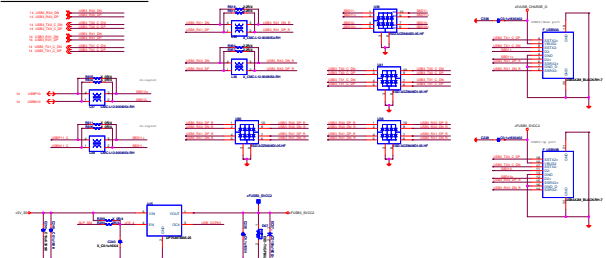


Pin	Signal	Function
1	VBUS	POWER
2	D-	DATA
3	D+	DATA
4	GND	GROUND

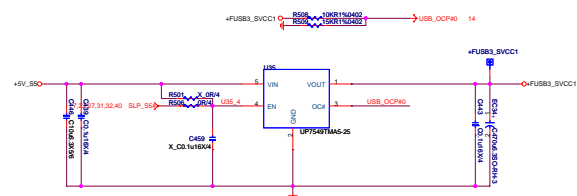
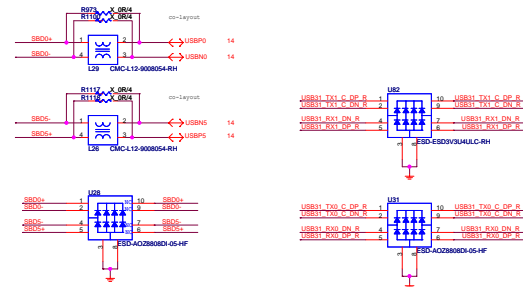
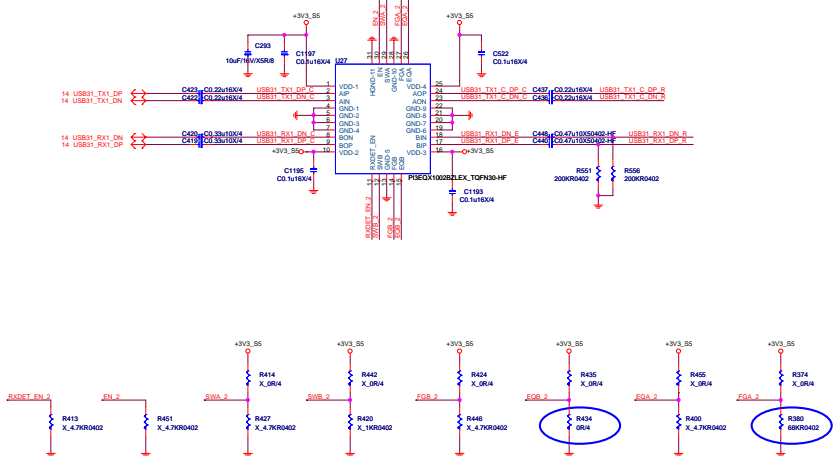
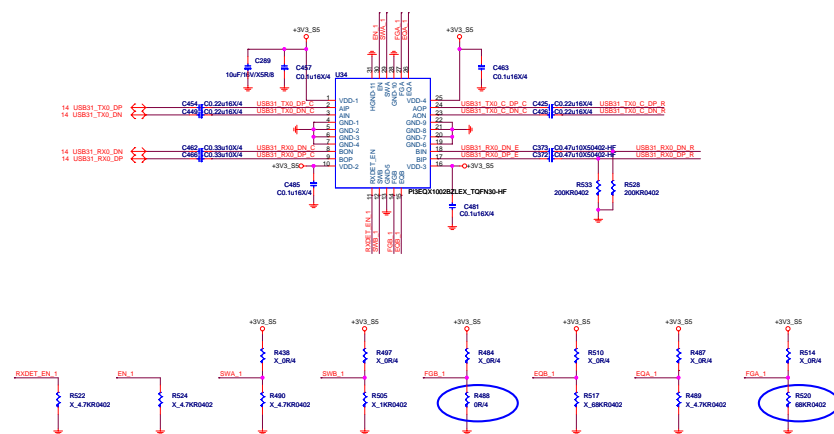
Rear USB Connector For USB Port 1/4



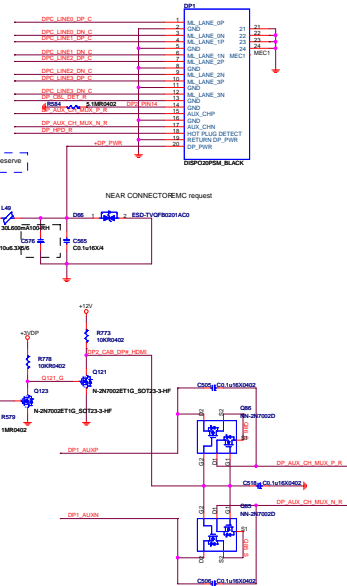
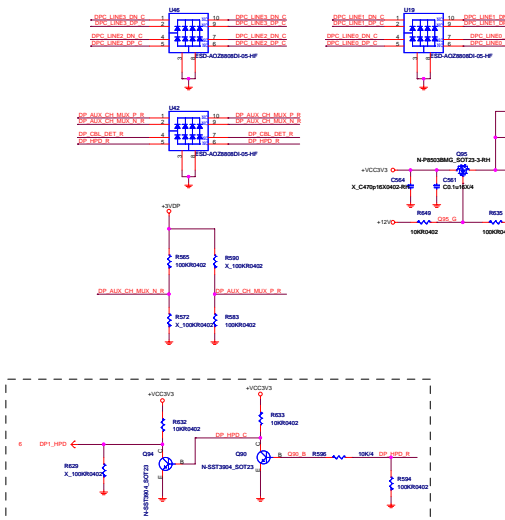
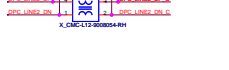
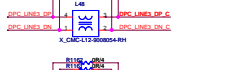
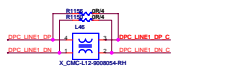
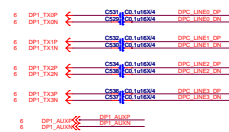
Front Panel USB Connector For USB Port 3/4



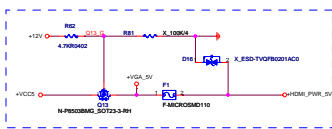
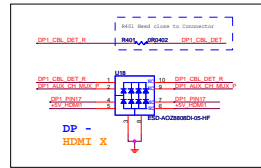
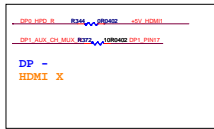
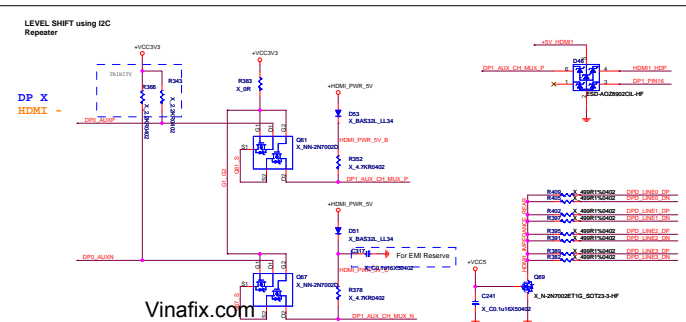
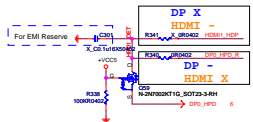
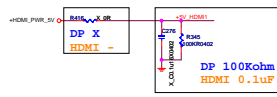
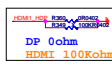
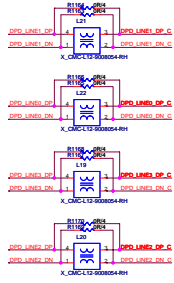
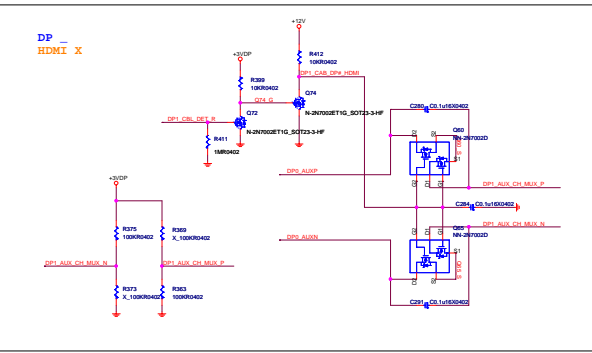
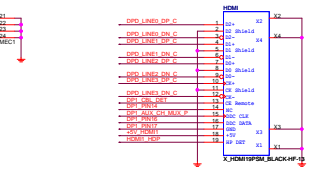
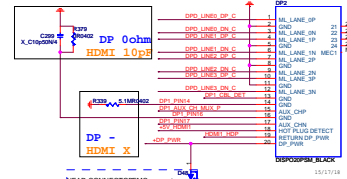
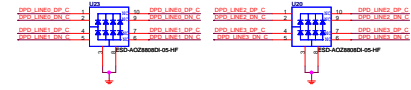
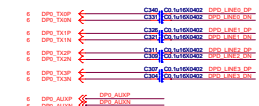
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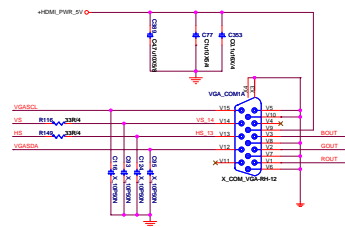
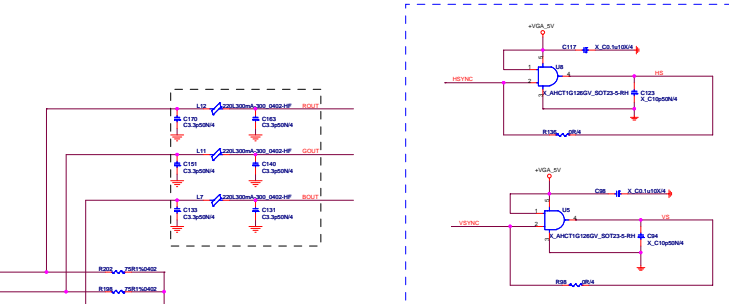
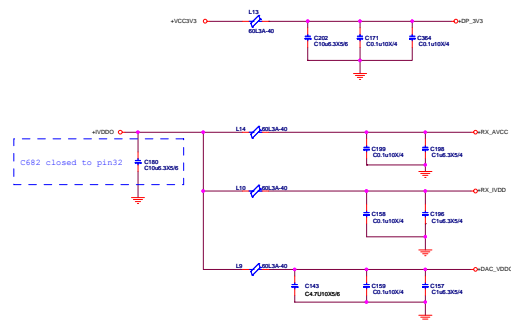


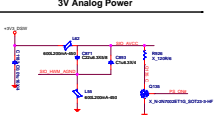
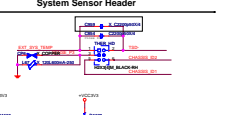
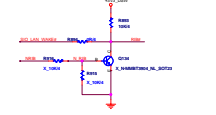
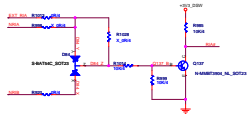
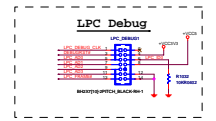
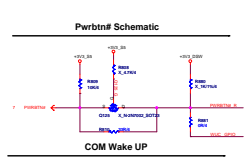
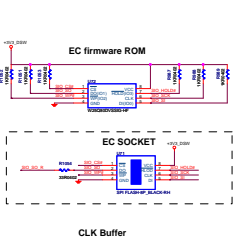
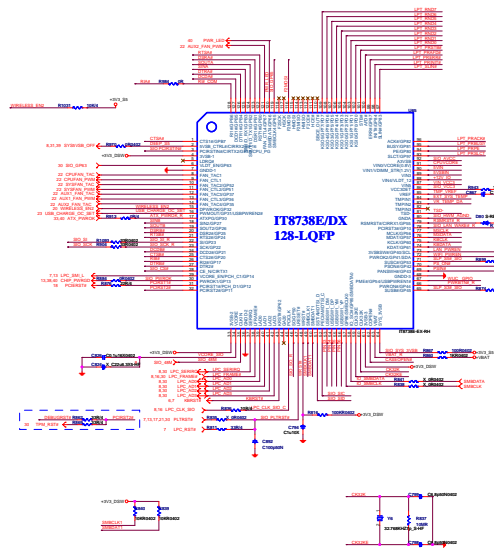
Display Port



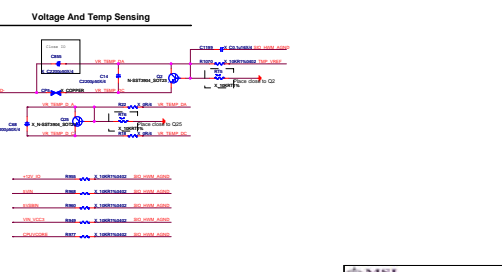
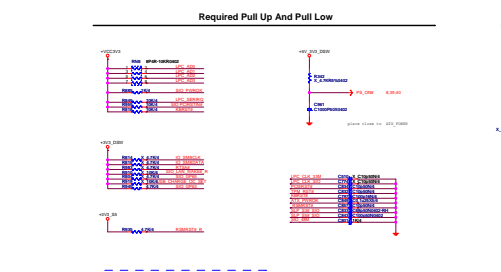
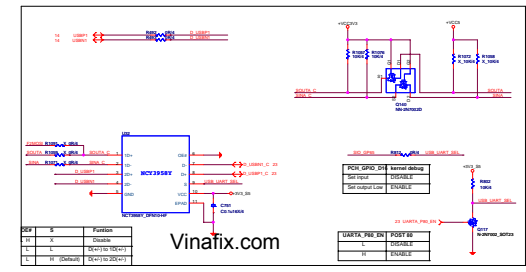
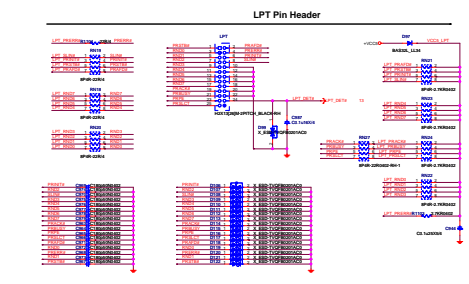
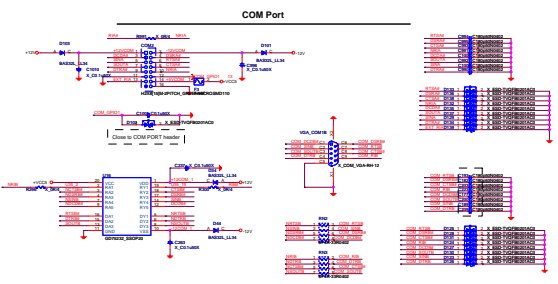
DP colay HDMI Port

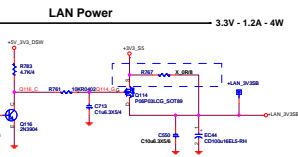
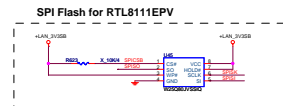
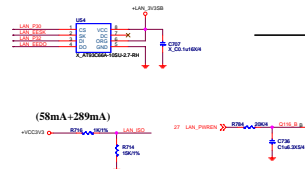
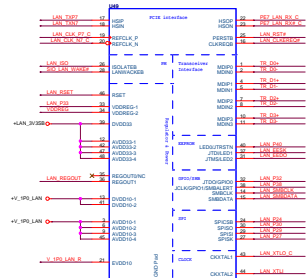
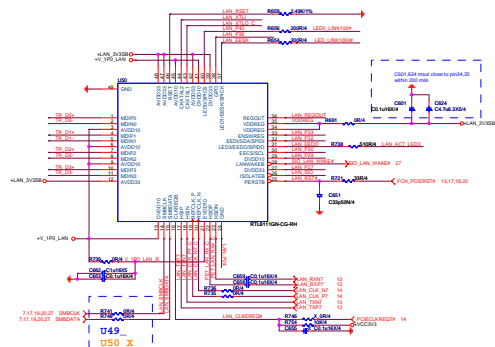






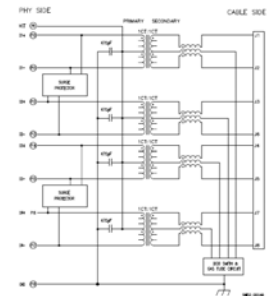
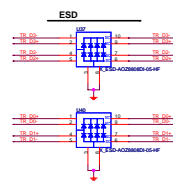
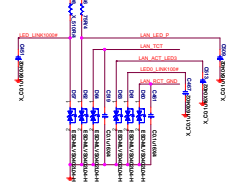
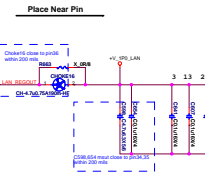
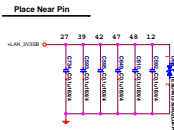
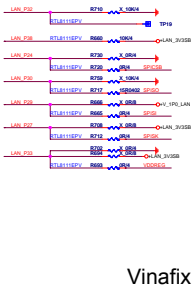
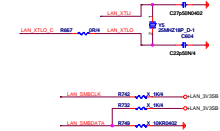
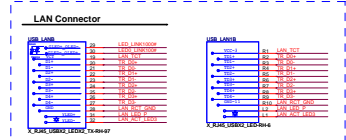
Pin	Signal	IO	IO	IO	IO
1	VCC	1	1	1	1
2	VCC	1	1	1	1
3	VCC	1	1	1	1
4	VCC	1	1	1	1
5	VCC	1	1	1	1
6	VCC	1	1	1	1
7	VCC	1	1	1	1
8	VCC	1	1	1	1
9	VCC	1	1	1	1
10	VCC	1	1	1	1
11	VCC	1	1	1	1
12	VCC	1	1	1	1
13	VCC	1	1	1	1
14	VCC	1	1	1	1
15	VCC	1	1	1	1
16	VCC	1	1	1	1
17	VCC	1	1	1	1
18	VCC	1	1	1	1
19	VCC	1	1	1	1
20	VCC	1	1	1	1
21	VCC	1	1	1	1
22	VCC	1	1	1	1
23	VCC	1	1	1	1
24	VCC	1	1	1	1
25	VCC	1	1	1	1
26	VCC	1	1	1	1
27	VCC	1	1	1	1
28	VCC	1	1	1	1
29	VCC	1	1	1	1
30	VCC	1	1	1	1
31	VCC	1	1	1	1
32	VCC	1	1	1	1
33	VCC	1	1	1	1
34	VCC	1	1	1	1
35	VCC	1	1	1	1
36	VCC	1	1	1	1
37	VCC	1	1	1	1
38	VCC	1	1	1	1
39	VCC	1	1	1	1
40	VCC	1	1	1	1
41	VCC	1	1	1	1
42	VCC	1	1	1	1
43	VCC	1	1	1	1
44	VCC	1	1	1	1
45	VCC	1	1	1	1
46	VCC	1	1	1	1
47	VCC	1	1	1	1
48	VCC	1	1	1	1
49	VCC	1	1	1	1
50	VCC	1	1	1	1
51	VCC	1	1	1	1
52	VCC	1	1	1	1
53	VCC	1	1	1	1
54	VCC	1	1	1	1
55	VCC	1	1	1	1
56	VCC	1	1	1	1
57	VCC	1	1	1	1
58	VCC	1	1	1	1
59	VCC	1	1	1	1
60	VCC	1	1	1	1
61	VCC	1	1	1	1
62	VCC	1	1	1	1
63	VCC	1	1	1	1
64	VCC	1	1	1	1
65	VCC	1	1	1	1
66	VCC	1	1	1	1
67	VCC	1	1	1	1
68	VCC	1	1	1	1
69	VCC	1	1	1	1
70	VCC	1	1	1	1
71	VCC	1	1	1	1
72	VCC	1	1	1	1
73	VCC	1	1	1	1
74	VCC	1	1	1	1
75	VCC	1	1	1	1
76	VCC	1	1	1	1
77	VCC	1	1	1	1
78	VCC	1	1	1	1
79	VCC	1	1	1	1
80	VCC	1	1	1	1
81	VCC	1	1	1	1
82	VCC	1	1	1	1
83	VCC	1	1	1	1
84	VCC	1	1	1	1
85	VCC	1	1	1	1
86	VCC	1	1	1	1
87	VCC	1	1	1	1
88	VCC	1	1	1	1
89	VCC	1	1	1	1
90	VCC	1	1	1	1
91	VCC	1	1	1	1
92	VCC	1	1	1	1
93	VCC	1	1	1	1
94	VCC	1	1	1	1
95	VCC	1	1	1	1
96	VCC	1	1	1	1
97	VCC	1	1	1	1
98	VCC	1	1	1	1
99	VCC	1	1	1	1
100	VCC	1	1	1	1



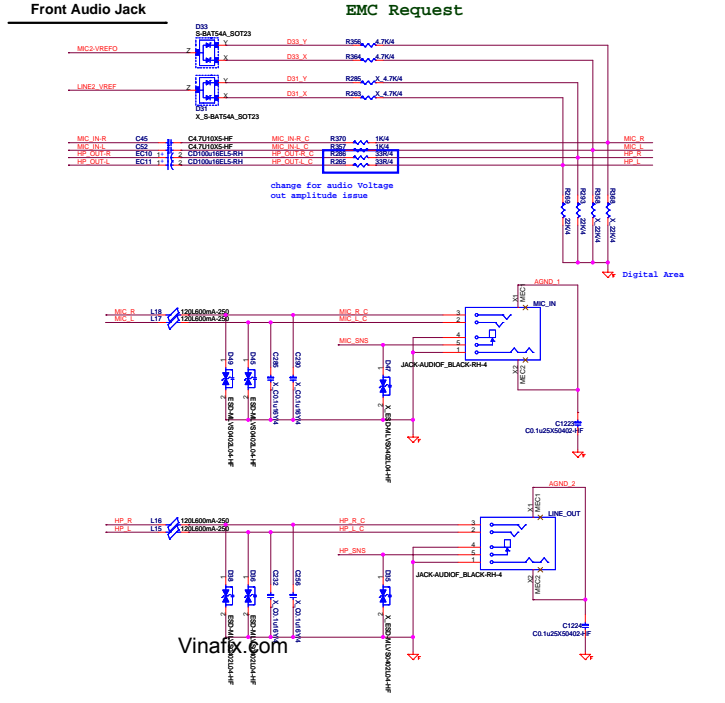
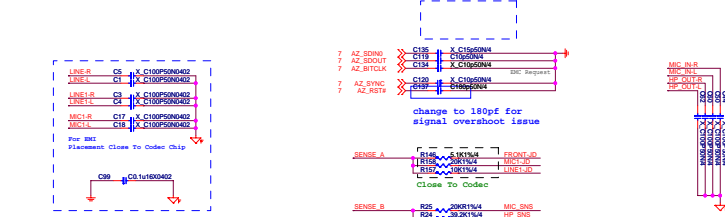


	LAM_FORCE	Q14_0	output	
is_fff_disabled	1	0	3.3V	
of_fff_disabled	0	1	0V	

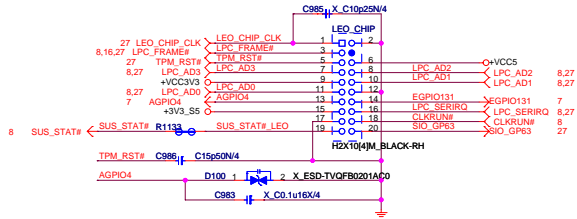
WOL	status	Yellow	Grn/On
don't care	No Link	off	off
off	S3/S4/S5	off	off
on	S3/S4/S5	off	off
on	10M inactive		off
on	10M active		off
on	100M inactive		
on	100M active		
on	1G inactive		
on	1G active		



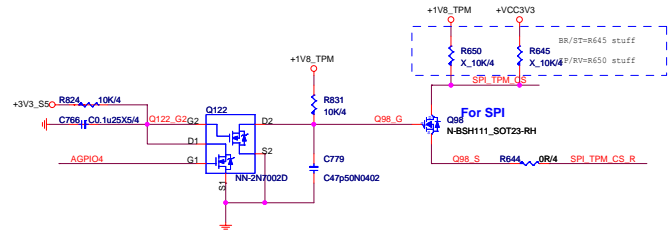
removed ALC662VC co-lay schematic on 0D



TCM Header

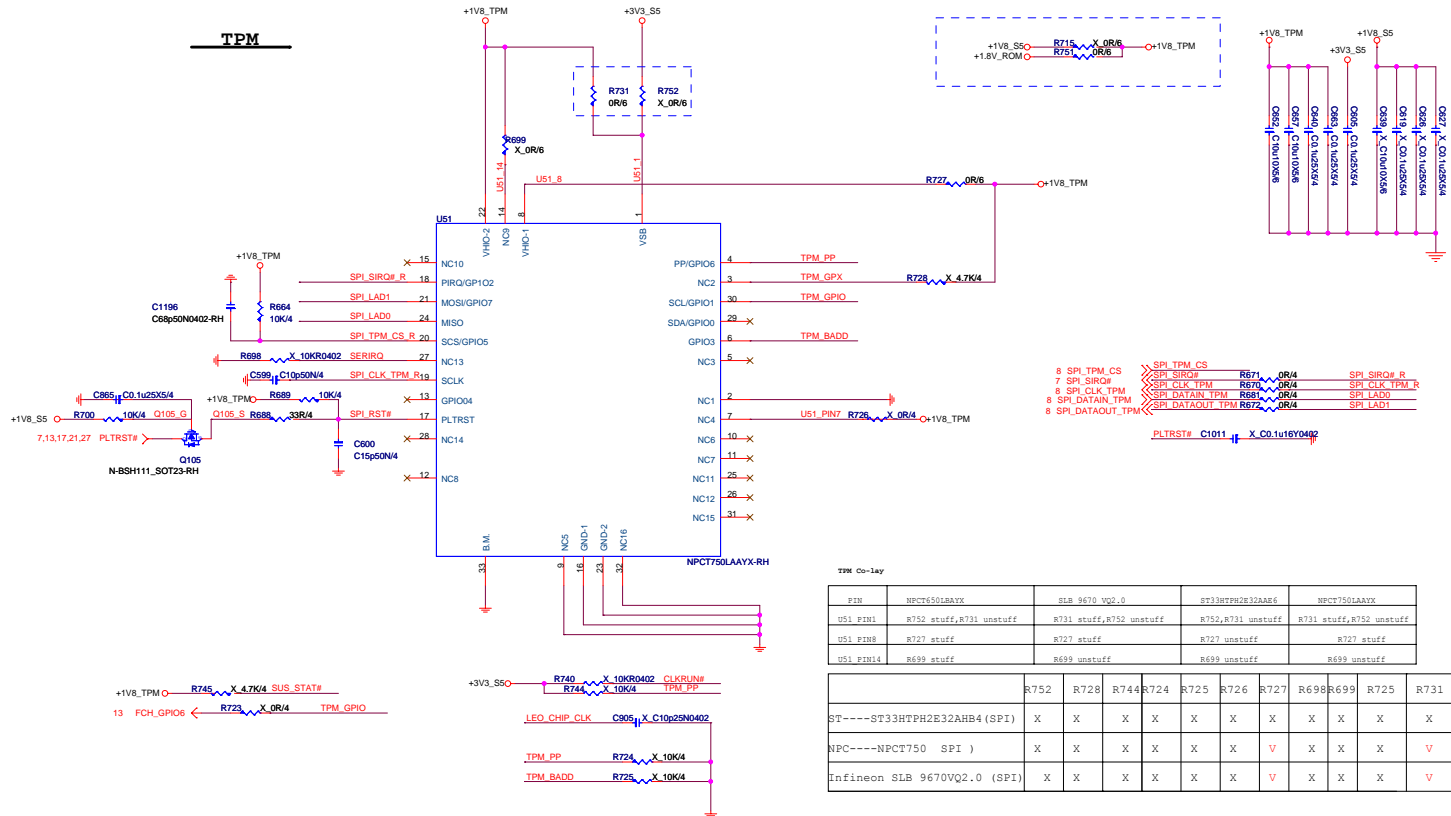


TPM disable circuit



AGPIO4	HIGH	LOW
TPM	ENABLE	DISABLE

TPM

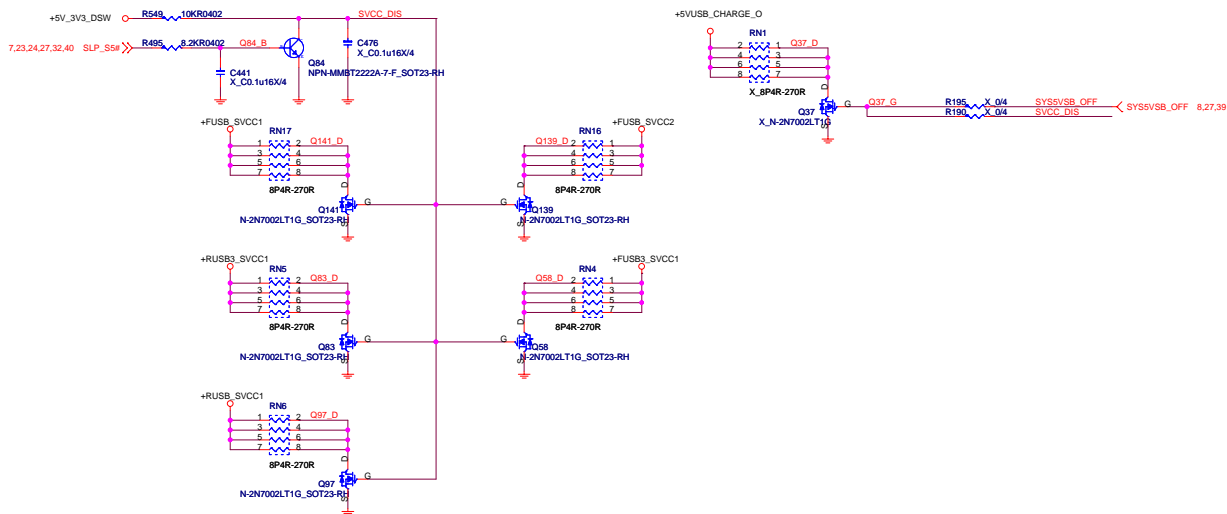


TPM Co-Lay

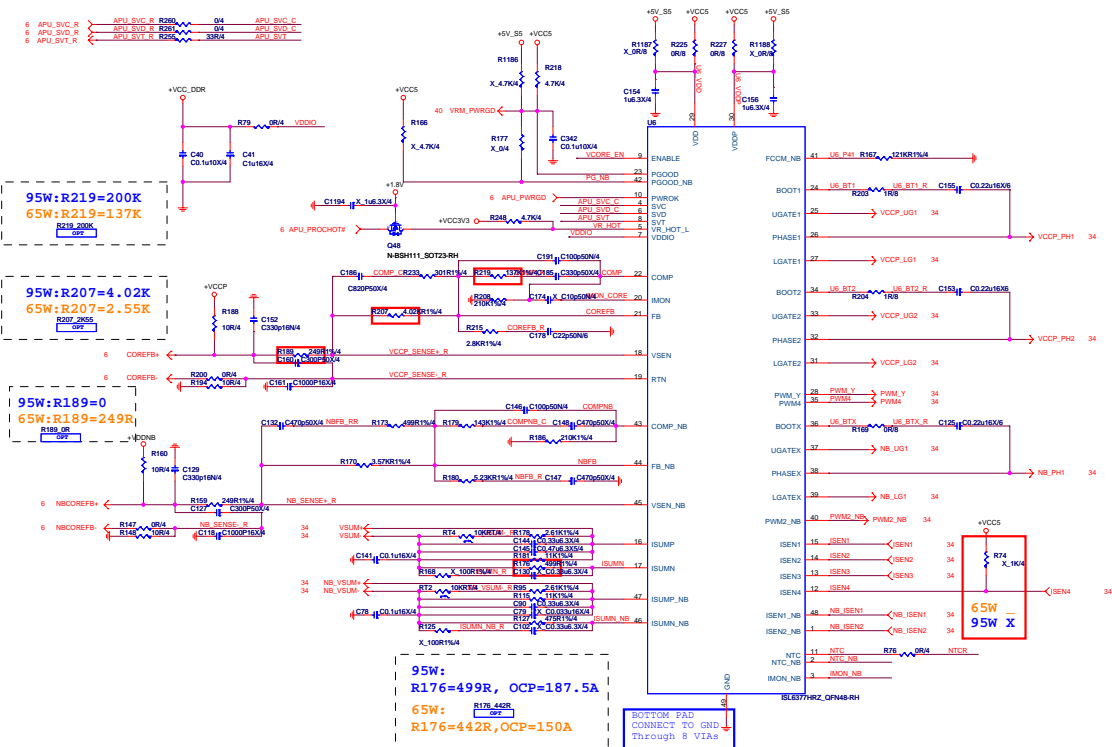
Pin	NPCT7501AAYX	SLB 9670 VQ2.0	ST33HTPH2E32AA66	NPCT7501AAYX
U51 PIN1	R752 stuff, R731 unstuff	R731 stuff, R752 unstuff	R752, R731 unstuff	R731 stuff, R752 unstuff
U51 PIN8	R727 stuff	R727 unstuff	R727 stuff	R727 stuff
U51 PIN14	R699 stuff	R699 unstuff	R699 unstuff	R699 unstuff

	R752	R728	R744	R724	R725	R726	R727	R698	R699	R725	R731
ST---ST33HTPH2E32AHB4 (SPI)	X	X	X	X	X	X	X	X	X	X	X
NPCT---NPCT7501 (SPI)	X	X	X	X	X	X	V	X	X	X	V
Infineon SLB 9670VQ2.0 (SPI)	X	X	X	X	X	X	V	X	X	X	V

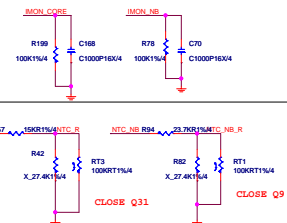
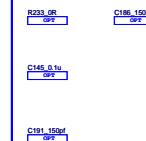
USB power discharge circuit



ISL6377HRZ
95W(A-Group) 4+2 Phase
65W(C-Group) 3+2 Phase



65W(SPECIAL)

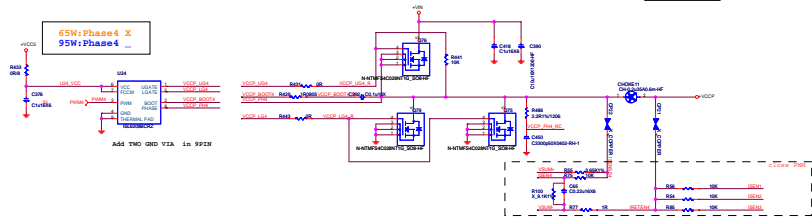
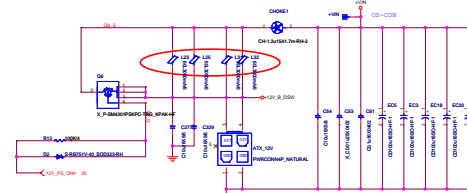
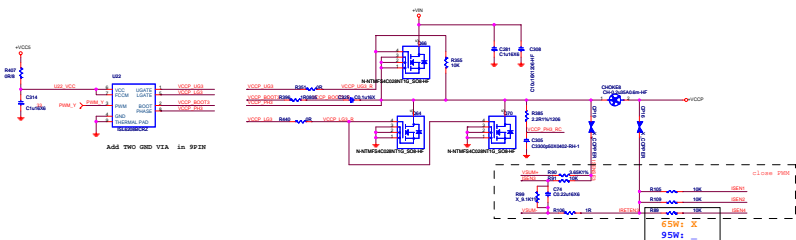
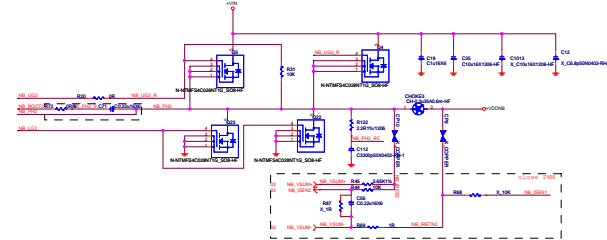
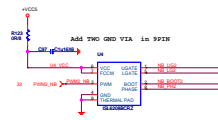
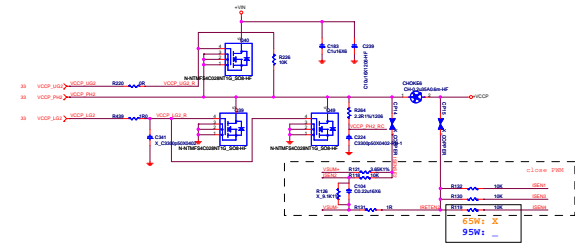
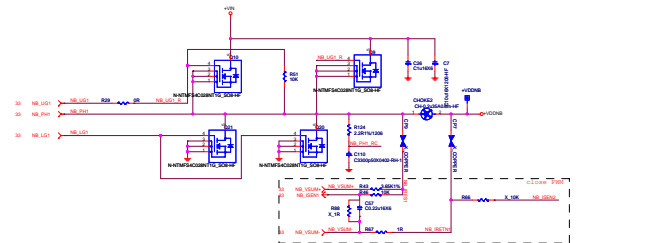
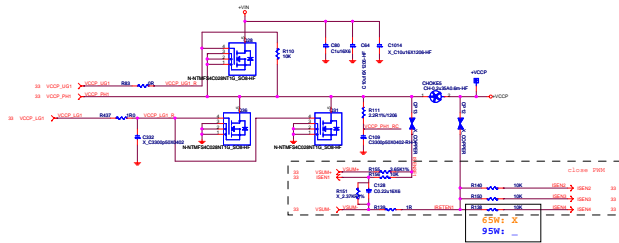


OTF:R735襪 襪N半祇



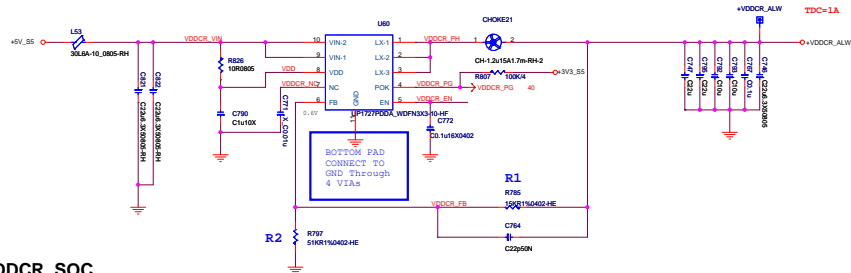
VCCP=0.75V-1.5V
95W(A-Group) TDC:80A, EDC:125A
65W(C-Group) TDC:65A, EDC:95A

VCCP_NB=0.75V-1.2V
95W(A-Group) TDC:30A, EDC:35A
65W(C-Group) TDC:50A, EDC:75A

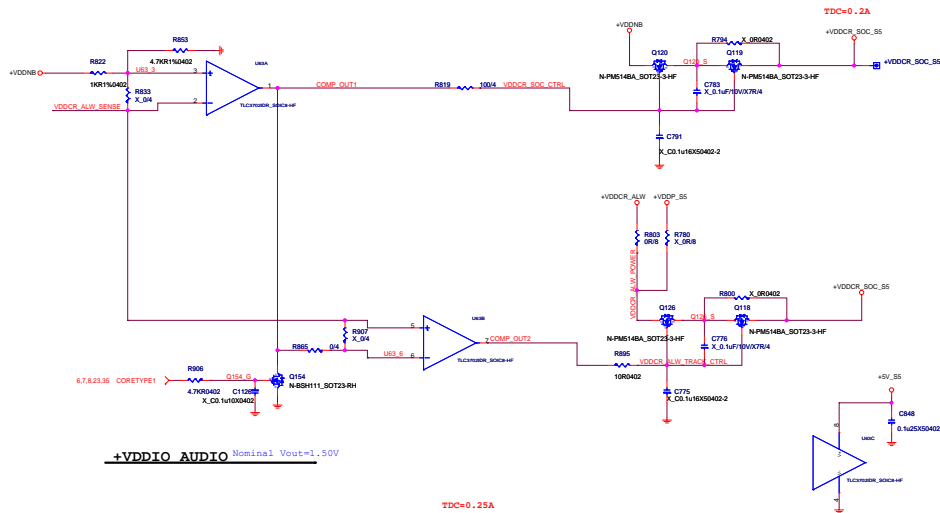


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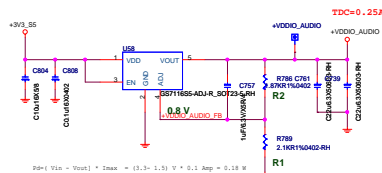
VDDCR_ALW



VDDCR_SOC



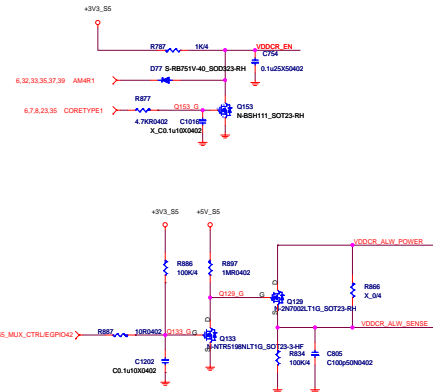
+VDDIO_AUDIO Nominal Vout=1.50V



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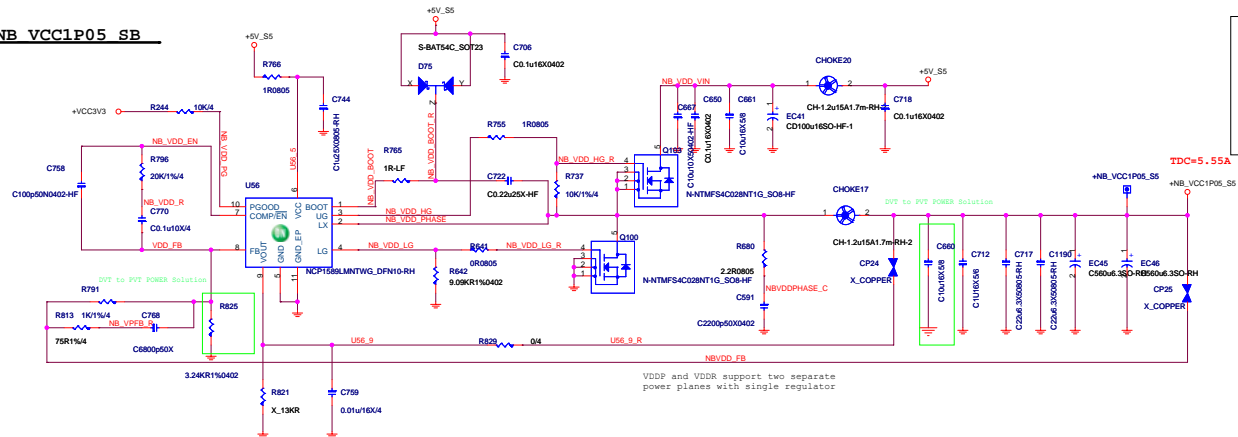
$V_O = 0.8 \cdot (R1 + R2) / R1$

Vd = 0.775V
Vta = 45V
Fd = 1000kHz
Current limit = 5-6A
Iout = 1A
L = 1.1uH/27A
Vio_Tmax = 0.35A
LIR = 409
Cio, CAP = 0.43uF
Cout_CAP = 11uF



State	s5_mux_ctrl1	s3#	s5#	VDDCR_SOC_S5 Voltage
G3	X	0	0	OFF
S5	0	0	0	ON(=+VDDCR_ALW)
S3	0	0	1	ON(=+VDDCR_ALW)
#0, but still in Reset	0	1	1	ON(=+VDDCR_ALW) or if VDDNB=+VDDCR_ALW, Tracks VDDNB
S0	1	1	1	Tracks +VDDNB

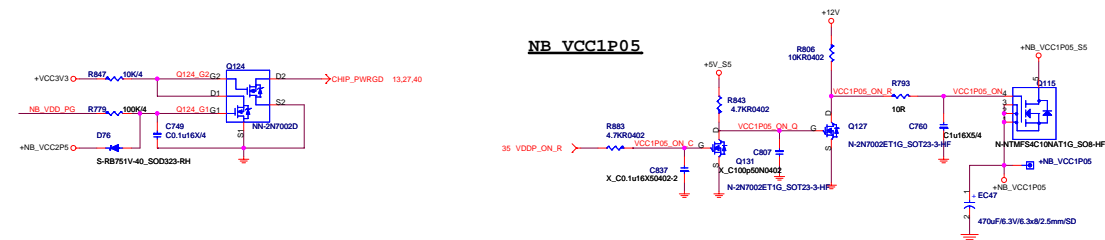
NB VCC1P05 SB



```
Vo =1.05V
Vin =5V
FS = 300khz
OCP 150%-200%
Iout =5.55A
L=1.1uH/27A
Vin Irms =2.26A
LIR=45%
Cin CAP =10.2uF
Cout CAP =223.3uF
```

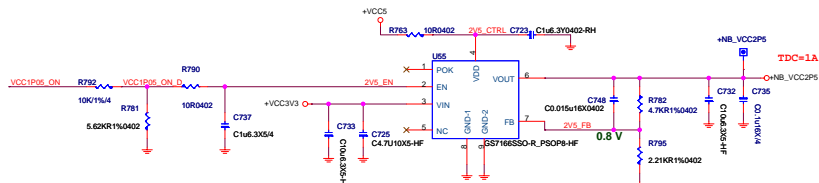
VDDP and VDDR support two separate power planes with single regulator

NB VCC1P05



NB VCCP2P5

$$\begin{aligned} V_{out} &= 0.8[(R_1+R_2)/R_2] \\ &= 0.8((4.7K+2.21K)/2.21K) \\ &= 2.5V \end{aligned}$$



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5V
19.5A

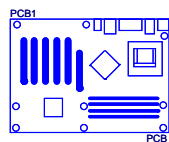


5V
19.5A

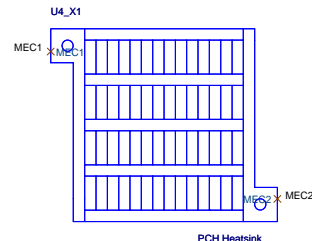
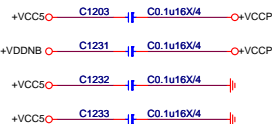


5V
19.5A

Manual Parts

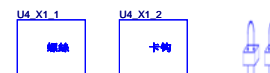
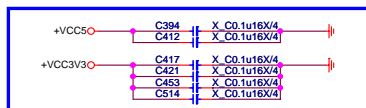
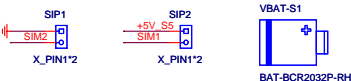


For AMD



PCH Heatsink

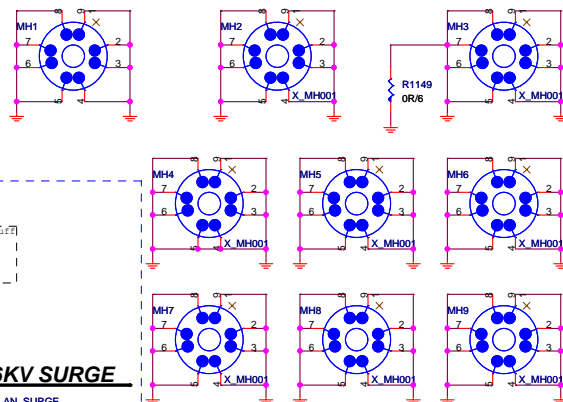
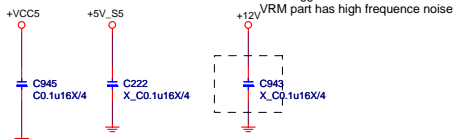
Simulation



Mounting Holes



For EMI



Optics Orientation Holes

Optical Fiducial Marks-120



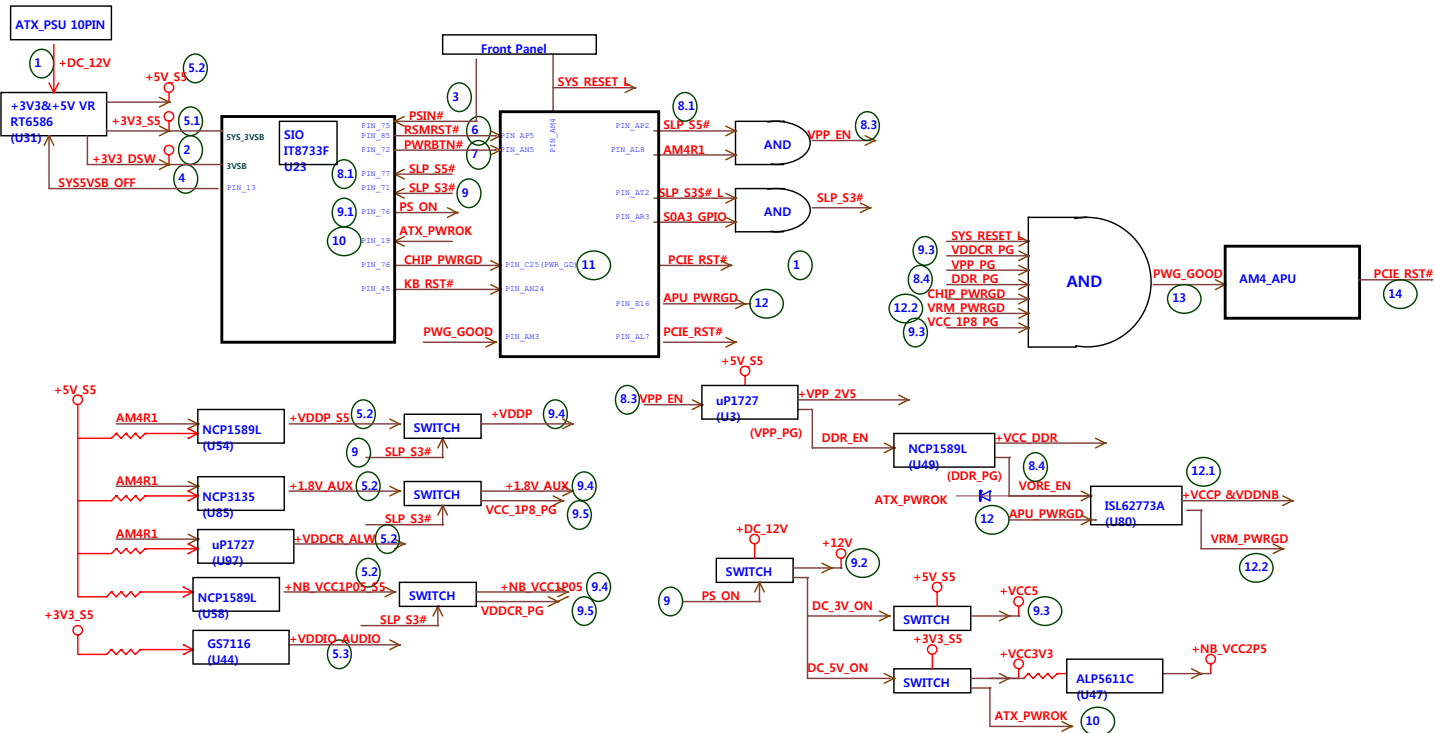
Without SURGE

With 6KV SURGE

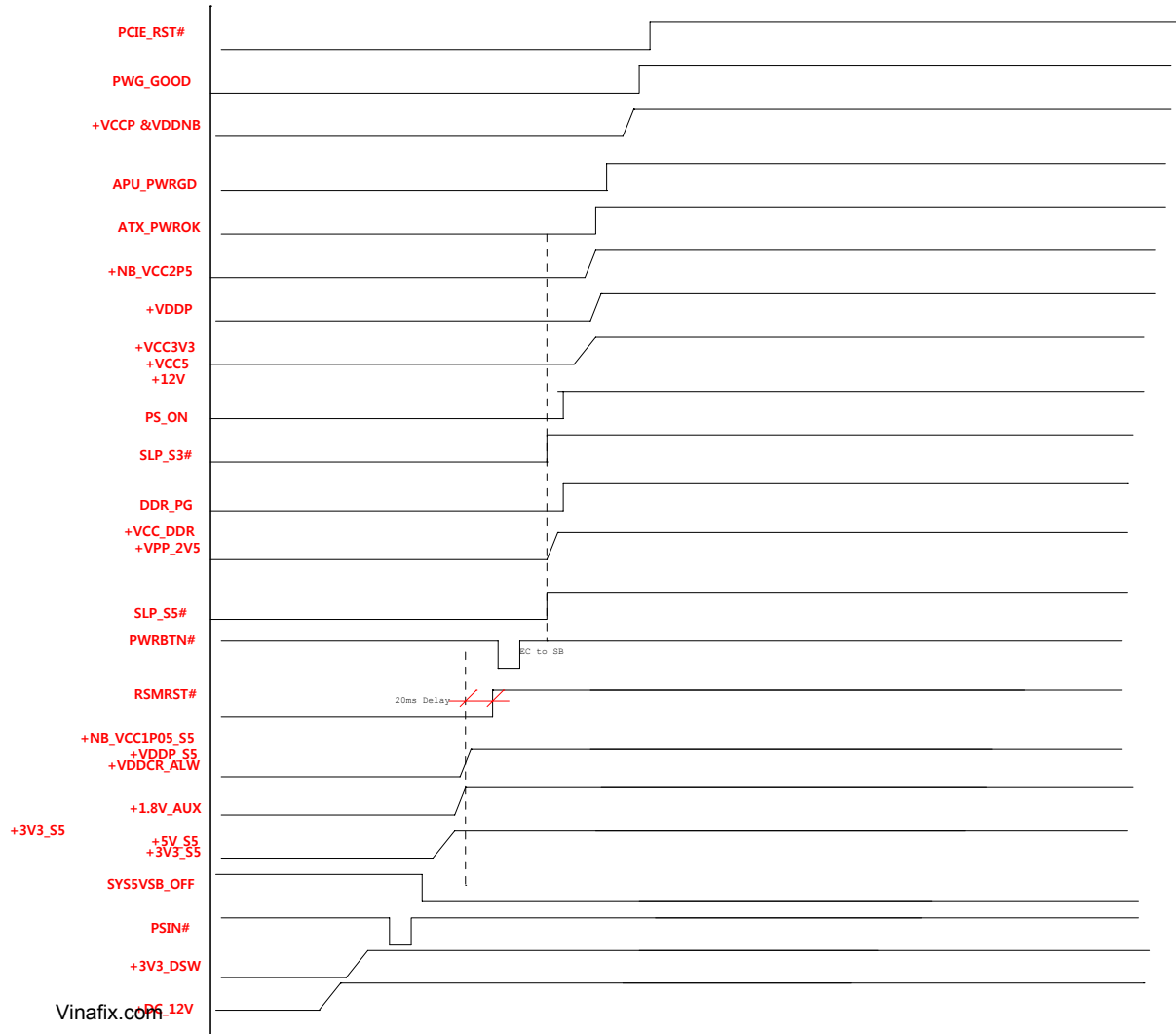
Reserve with surge single LED

MICRO-START INTL CO.,LTD		
Title Manual & Option Parts		
Size	Document Number	Rev
	MS-7C26	1.0
Date:	Wednesday, May 29, 2019	Sheet 41 of 47

Power Sequence Diagram



Power Sequence Timings



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PN	OPN	Name	Default	Define	Signal Name V.I.	Setting V.I.
AT23	OP1000	CIA_RNGD_L/ATA110_L/ATA1_IP1_L/ATP100	OP1	OP10	CNR_OP101_T00T	TP Fcvti Adivsion opn to receive RINGD/ATA100
AT24	OP1010	CIA_RNGD_L/ATA110_L/ATA1_IP10	OP1	OP10	LPT_T00T_T00T	TP Fcvti Adivsion opn to receive RINGD/ATA100
AT26	OP1010	CIA_RNGD_L/ATA110_L/ATA1_IP10	OP1	OP10	CNR_L/ATA10010	OP1 (C) 100 Select
AT27	OP1010	CIA_RNGD_L/ATA110_L/ATA1_IP10	OP1	OP10	RNGD_OP1010	TP Fcvti Adivsion opn to receive RINGD/ATA100
AR22	OP1010	CIA_RNGD_L/ATA110_L/ATA1_IP10	OP1	OP10	RNGD_OP1010	TP Fcvti Adivsion opn to receive RINGD/ATA100

PCN	QF10	Name	Default	Defcon	Signal Name V1.0	Setting V1.0
B0	QF100	QF100	QF100	QF100	PCB 402744 QF10.0	PCB 410001 175
B0	QF100	QF101	QF101	QF101	PCB 410001	PCB 410001 175
B0	QF100	QF102	QF102	QF102	PCB 410001	PCB 410001 175
B0	QF100	QF103	QF103	QF103	PCB 410001	PCB 410001 175
B0	QF100	QF104	QF104	QF104	PCB 410001	PCB 410001 175
B0	QF100	QF105	QF105	QF105	PCB 410001	PCB 410001 175
B0	QF100	QF106	QF106	QF106	PCB 410001	PCB 410001 175
B0	QF100	QF107	QF107	QF107	PCB 410001	PCB 410001 175

[illegible]

API	QF30		Default	Defcon	Transit Mode V1.0	Building V1.0
AMA	QF000	STS, REBT, LAMP105	QF100P0	QF1	STS, REBT, L	
AL7	QF1024	PAIR, LAMP105	QF010	QF1	PAIR, REBT, L	
AN2	QF000	POB, LAMP105	QF010	QF1	POB, REBT, L	
AL5	QF000	POB, LAMP105	QF1	QF01		POB, L
QF1011	SLINKY, INCT, L		QF010	QF0		POB, L
AN24	QF10024	REBT, LAMP105	QF1	QF000T, L	REBT, L	
QF1040		IN, CHL, CHL2	QF100P0	QF0	IN, MIX, CHL7, REBT7/1042	QF1 (CHL7, 70.5 & 1.0)
AP3	QF000	QNA3, LAMP105	QF100P0	QF0	QNA3, QF20	

PCN	SPID	Base	Default	Define	Signal Name V1.0	Setting V1.0
A1	SP10.R0	SP10.R0	QF1AQPO	QPO	SP1_CAD_SP_MON10	SP/ROM0 CTL
B0	SP10.R1	SP10.R1	QF1AQPO	QPO	SP2_CAD_SP_MON10	SP/ROM0 CTL
A4	SP10.R0	SP10.R0	QF1AQPO	QPI	CRAS115_101	QPI
C1	SP10.R1	SP10.R1	QF1AQPO	QPI	CRAS115_101	QPI

Item	QFN	Pin Count	Ref(sell)	Ref(sup)	Signal Rate T1.0	Setting T1.0
ALI	QF0016	20B, 0.1/0.16	QFI	QFI	WIRELESS_001	QFI External Pull High
ALI	QF0017	20B, 0.1/0.17 ACF0151	QFI	QFI	WIRELESS_001	QFI External Pull High
ALI	QF0018	20B, 0.1/0.18 ACF0151	QFI	QFI	QFI_0F011	QFI External Pull High
API	QF0019	20B, 0.1/0.19 ACF0151	QFI	QFI	QFI_0F019	QFI External Pull High

[illegible]

Pin	GPIO	Name	Default	Define	Signal Name V1.0	Setting V1.0
AW23	GPIO0	SPER/AGP001	GPIO	SPER	SPER	SPER

PCN	QID	Base	Default	Define	Signal Base V.L.0	Setting V.L.0
AT25	Q10113	SC1/17323_SC1/ RSP17323	Q1/1200	000	200C13_000	SC10
AK3	Q10109	SC1/17323_SC1/ADP10109	Q1/1200	000	200C10_000	SC13
AS25	Q10114	SC1/17323_SC1/ RSP17323	Q1/1200	000	200C14_000	SC10
Q1	Q10100	SC1/17323_SC1/	Q1/1200	000	200C10_000	SC10

PCN	CP10	Name	Default	Define	Signal Name V1.0	Setting V1.0
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PN	QPID	Name	Default	Define	Signal Name V1.0	Setting V1.0
AX18	QPID10	LPCFMR1/REF10109	QPS	LPC	LPC_FMR18A	LPCFMR_1
AX19	QPID9	LPCCLDR1/LPC10109	QPS	LPC	LPC_CLDR1	LPCCLDR_1
AX19	QPID15	LPCCLDR1/REF10105	QPS1000	LPC	LPC_CLDR1	LPCCLDR_1
AX19	QPID100	LPC_CLDR1/REF10100	QPS	LPC	LPC_CLDR100A	LPCCLDR_1
AX19	QPID101	LPC_PD1/REF10101	QPS	LPC	REF10101	LPC_PD_1
AX2	QPID2	LPC_FMR1/REF10102	QPS	LPC	LPC_FMR1	QPS High

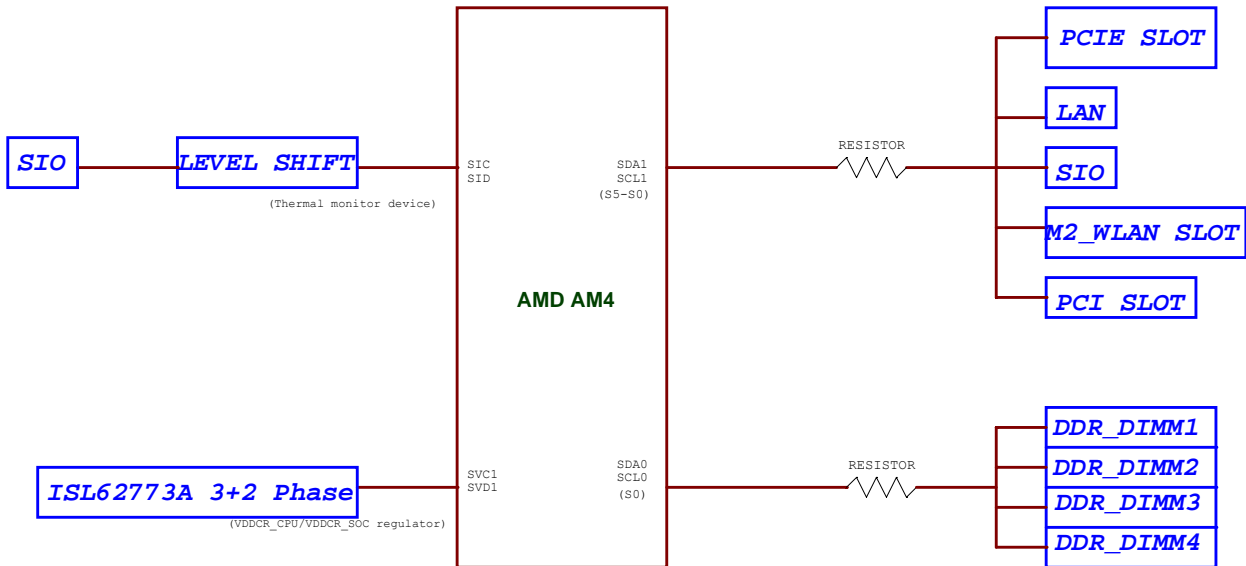
B21	CP10_R14	CP10_R14/PRODUCT	CP1/CP0	CP1	BR_333	BIN_OPTION
A21	INT_CP10	INT_CP10/PRODUCT	CP0	CP1	FW_INT	FW_INT

PCN	QPN	Base	Default	Define	Signal Name V.L.O	Setting V.L.O
AT20	Q110104	LAD1/NEP110104	Q110104	LPC	LPC_A00	LAD0
AT21	Q110105	LAD2/NEP110105	Q110105	LPC	LPC_A01	LAD1
AT22	Q110106	LAD3/NEP110106	Q110106	LPC	LPC_A02	LAD2
AT23	Q110107	LAD4/NEP110107	Q110107	LPC	LPC_A03	LAD3
AT24	Q110107	SRB1/NEP110107	SRB	SRB1Rq	SRB_1SRBq	SRB1Rq

[illegible]

PIN	QFID	Name	Default	Define	Signal Name V1.0	Setting V1.0
AEV7	SP1009	SP1_TPM_CS_L1 M22E15	QF1/QF0	SP1_TPM_CS_L1	SP1_TPM_CS	SP1_TPM_CS_L1

PN	SPID	Name	Default	Define	Signed Name V1.0	Setting V1.0
AP13	021004	FAB13S/ACF1004	SP1	CP13	ACF1004	TP Point Obeisn guide no require 01004/1000
AP15	021005	FAB015S/ACF1005	CP0	CP15	FAB015T0	TP Point Obeisn guide no require 01005/1000
RE15	051004	AP1066/ DET000N_1	SP1/SP0	SP1	AP15_PROCT016	DET000N_1



RESET MAP

